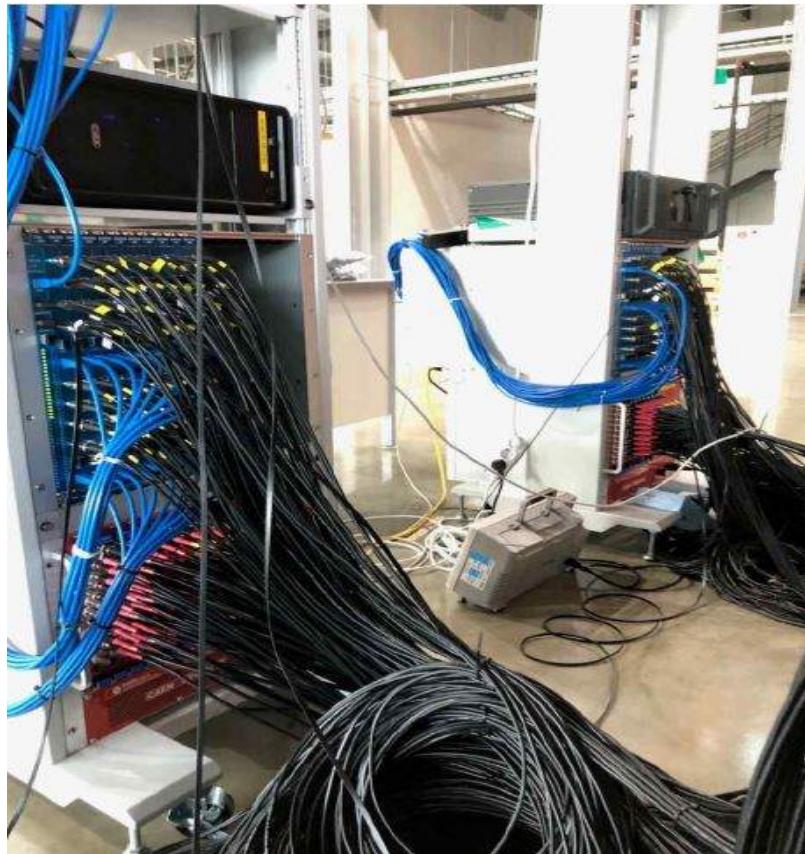


# 2026 검출기 워크샵

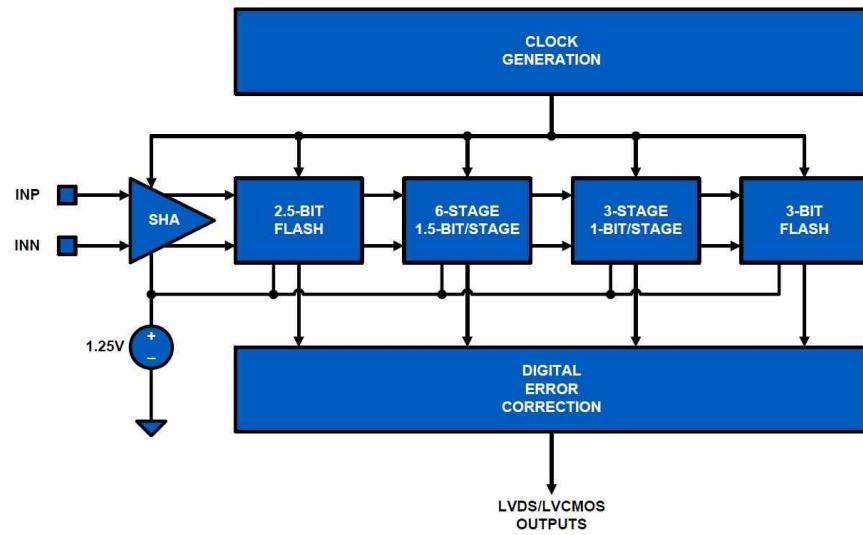
## Flash ADC Data AQuisition



김상열

**NOTICE** (주)노티스

# Flash ADC



➤ We call Flash ADC(FADC) when ADC has sampling rate more than 10 MHz.

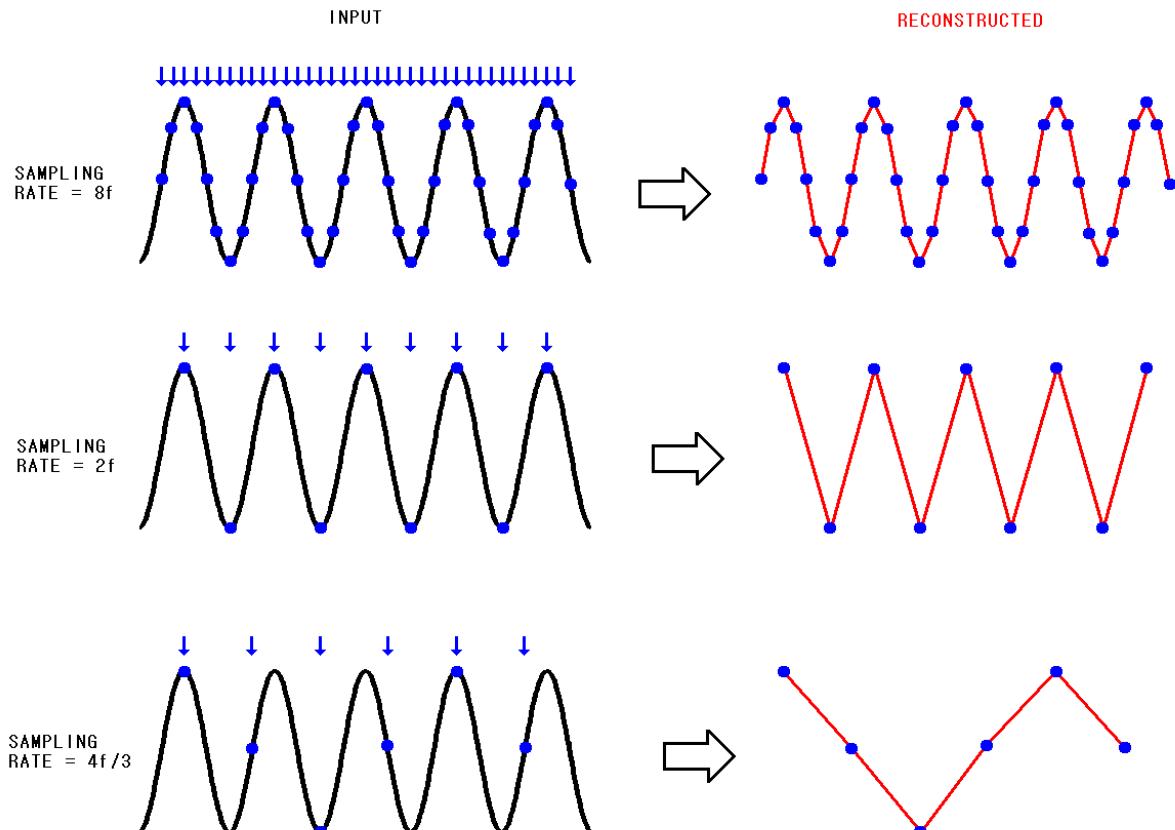
But most of them are pipelined ADC.

Beside complex structure inside ADC IC, using it is very simple.

Applying analog input and sampling clock then we get digital data every clock cycle.

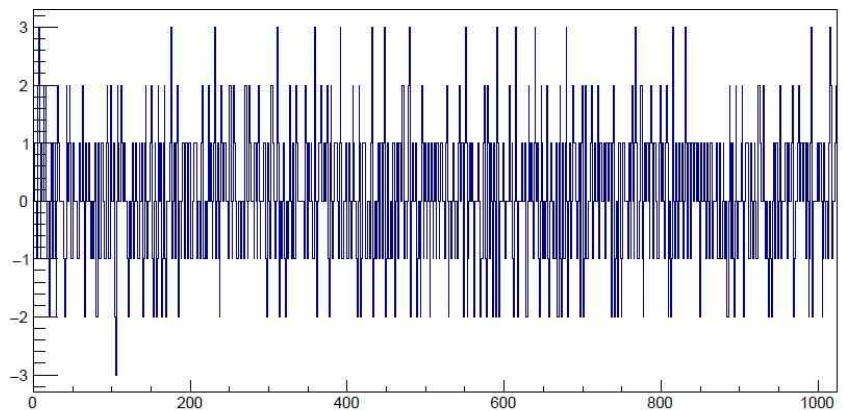
# Flash ADC specification 1

## Sampling rate

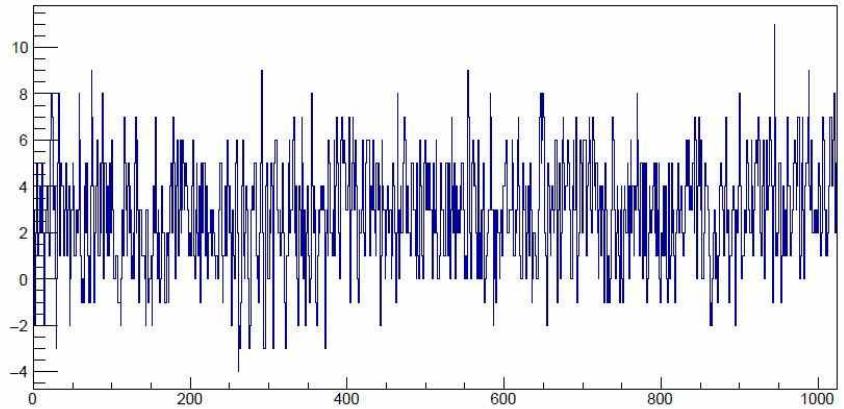


## Resolution (# of bits)

12 bit 500MSa/s



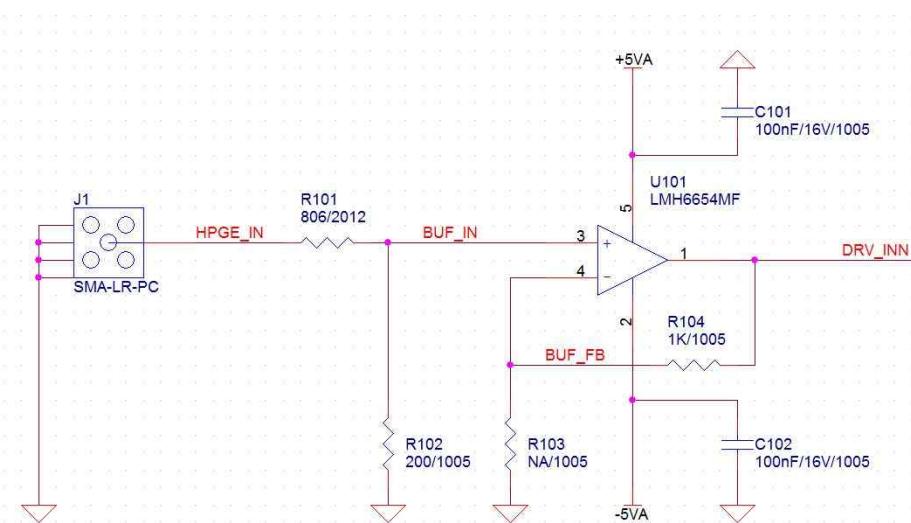
14 bit 500MSa/s



Real resolution = Effective # of bits(ENOB)  
SNR(Signal/Noise) =  $6.02 \times \text{ENOB} + 1.76$

# Flash ADC specification 2

Input voltage range



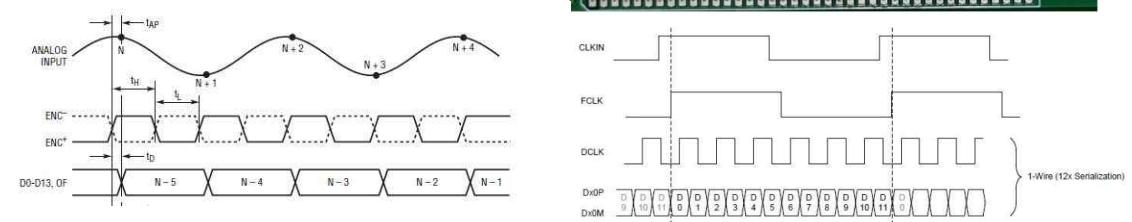
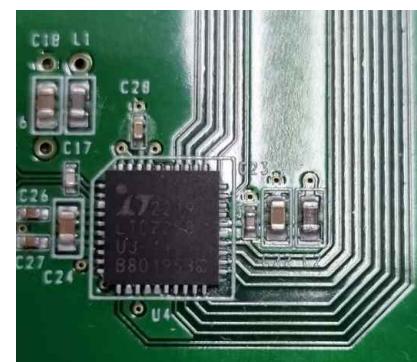
Usually 2Vp-p.

We attenuate or amplify input signal for ADC.

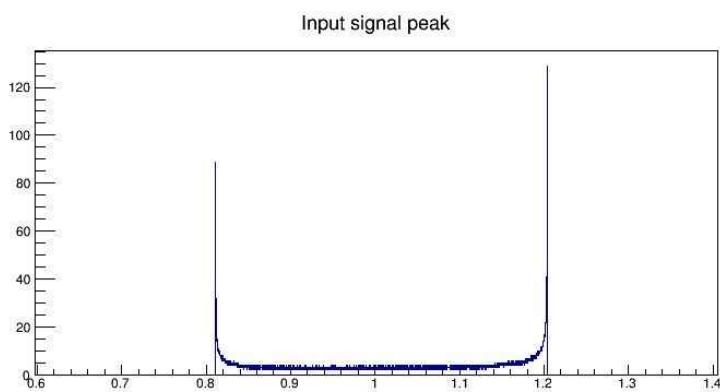
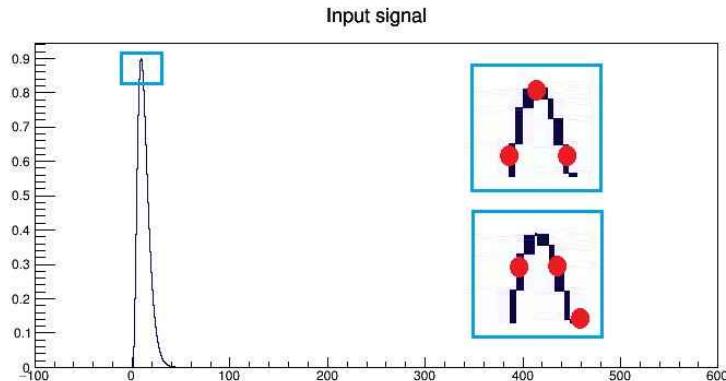
?? T better than A ??

- Input Analog Bandwidth  
Most ADC has larger bandwidth than  $\frac{1}{2}$  of maximum sampling rate.  
Okay except special design such as interleaving.

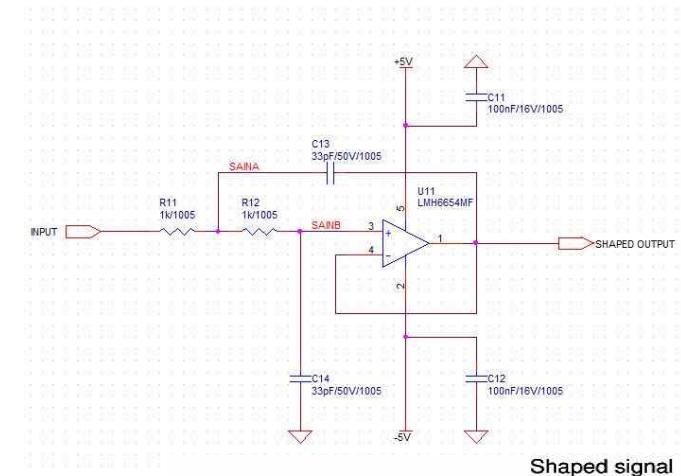
- Power consumption  
Newer = lower  
Low power supply voltage = lower
- # of channels = more the better



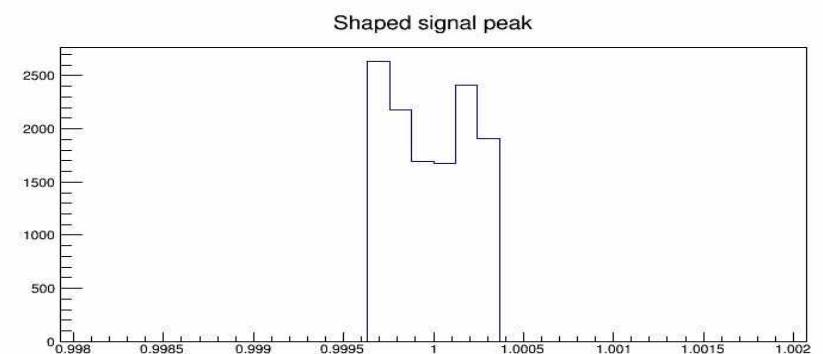
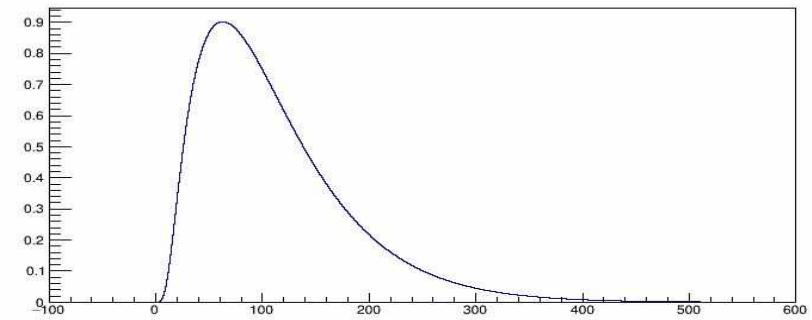
# Lowering ADC Sampling rate!



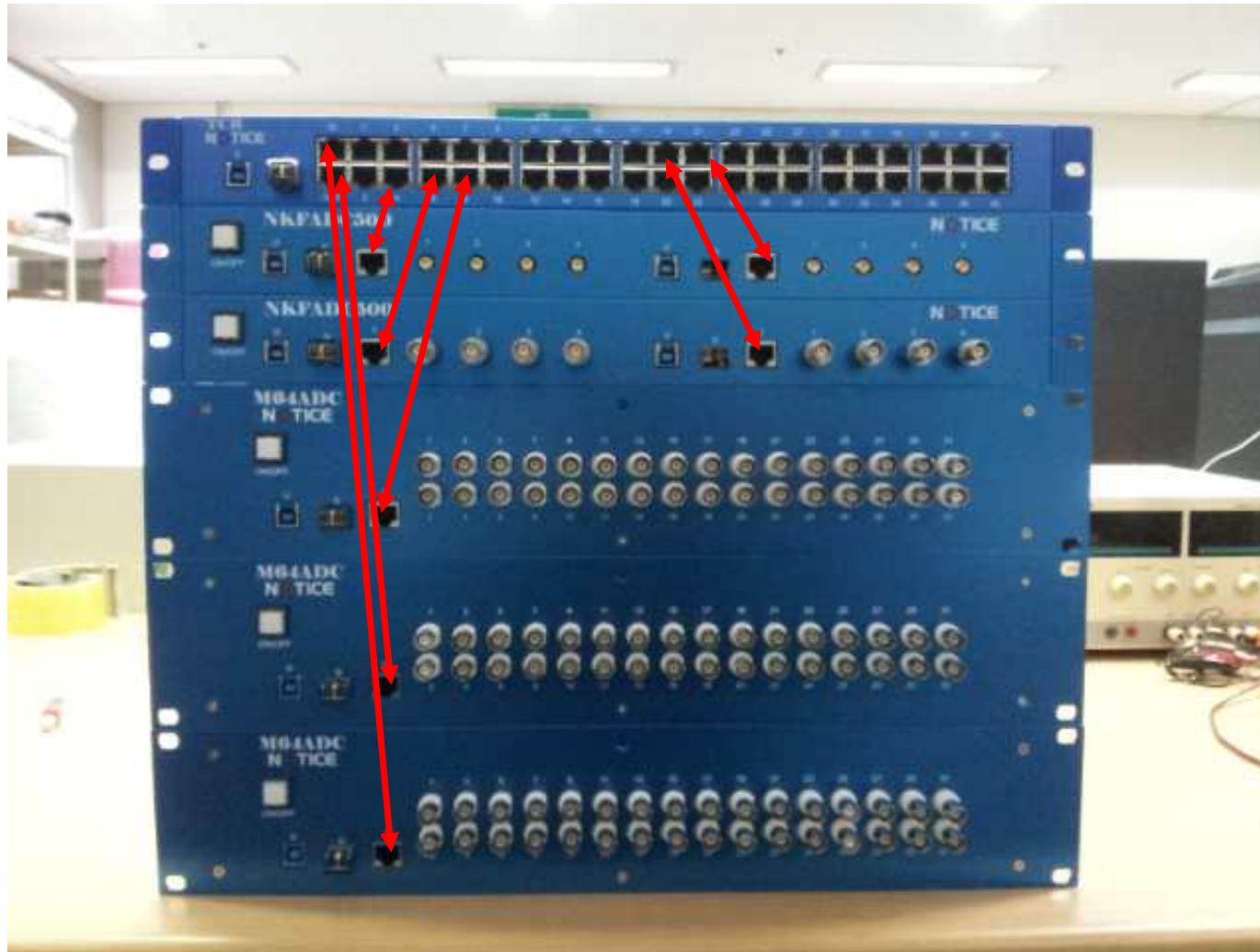
Problem with lower sampling rate  
(Input and ADC sampling is asynchronous)



Use low pass filter

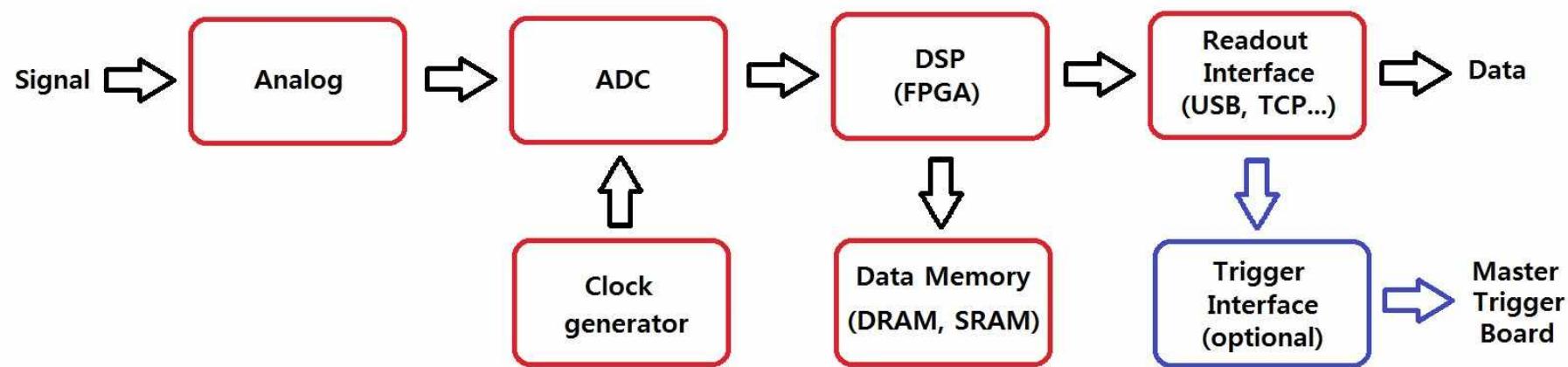
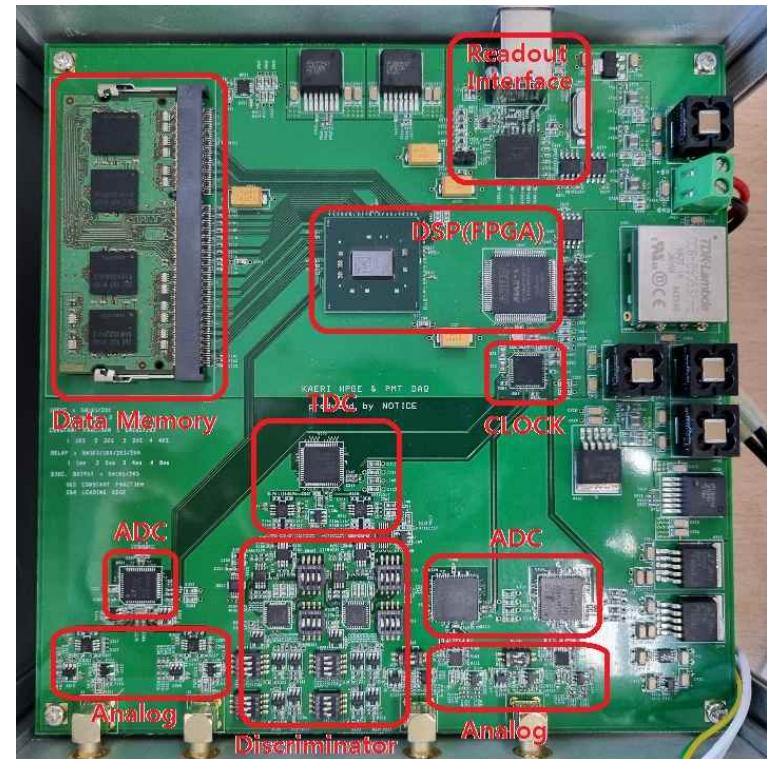


# Flash ADC trigger

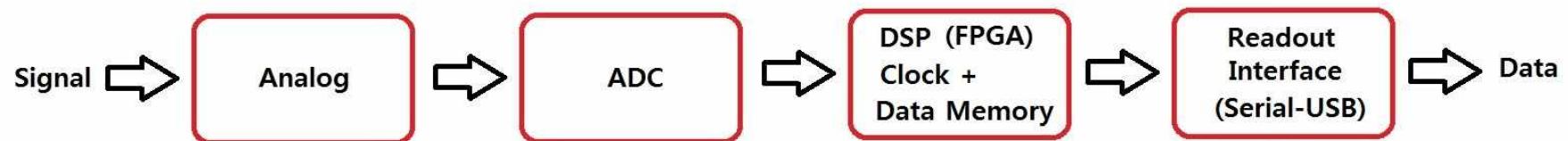
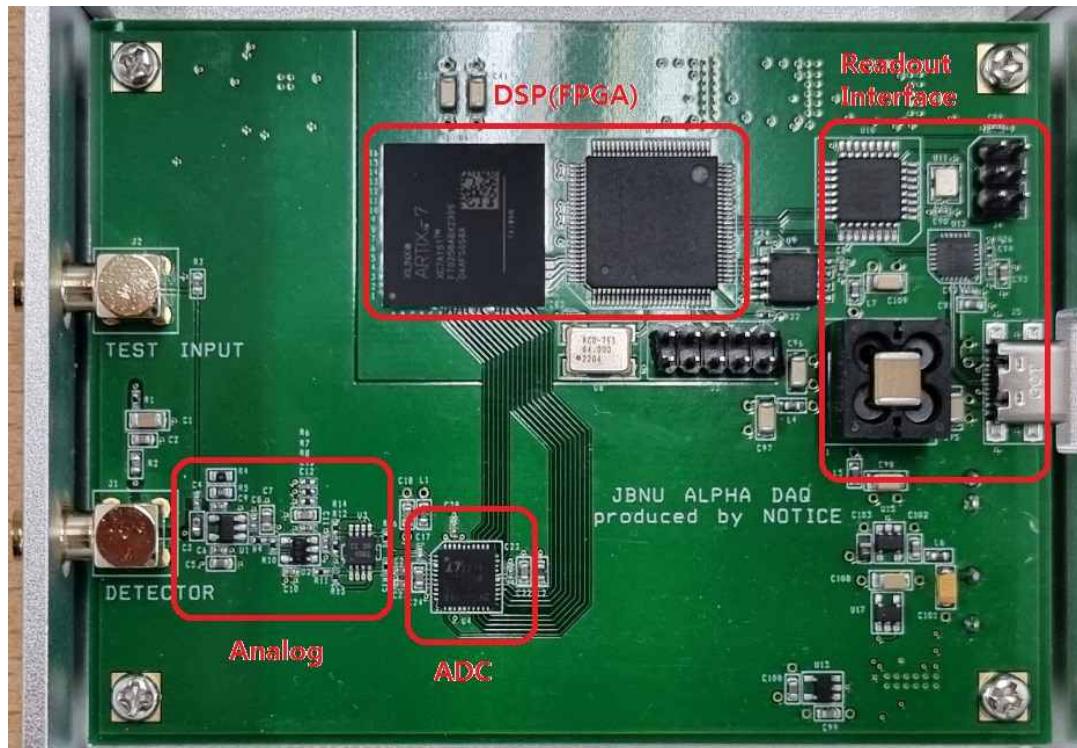


- ADC -> Trigger board  
Local trigger information  
(such as # of hit ch...)
- Trigger board -> ADC  
Global trigger information  
-> ADC stores data
- ADC should have enough FIFO  
memory that storing ADC data  
for trigger latency time.  
(Trigger latency can be  
sometimes more than 10 us)
- Trigger decision logic is  
designed in pipe-lined style  
to avoid dead-time.

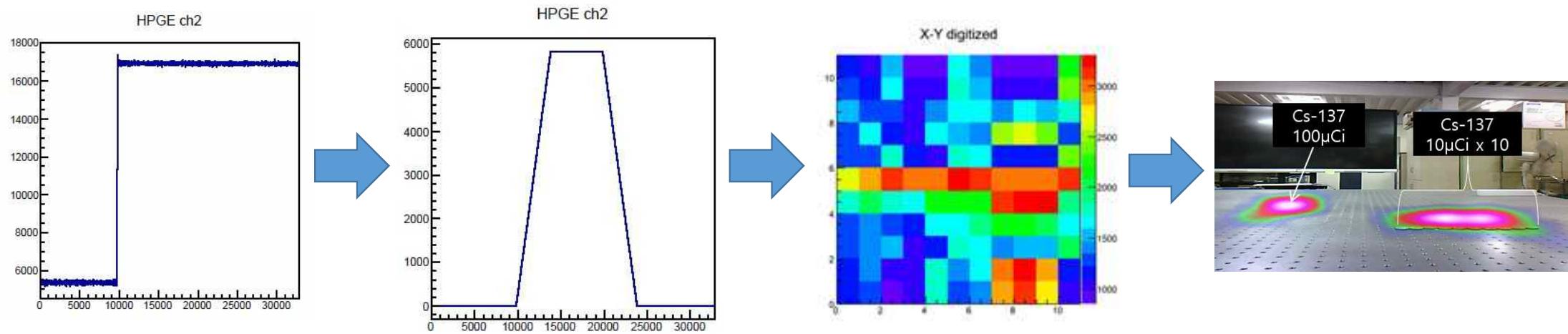
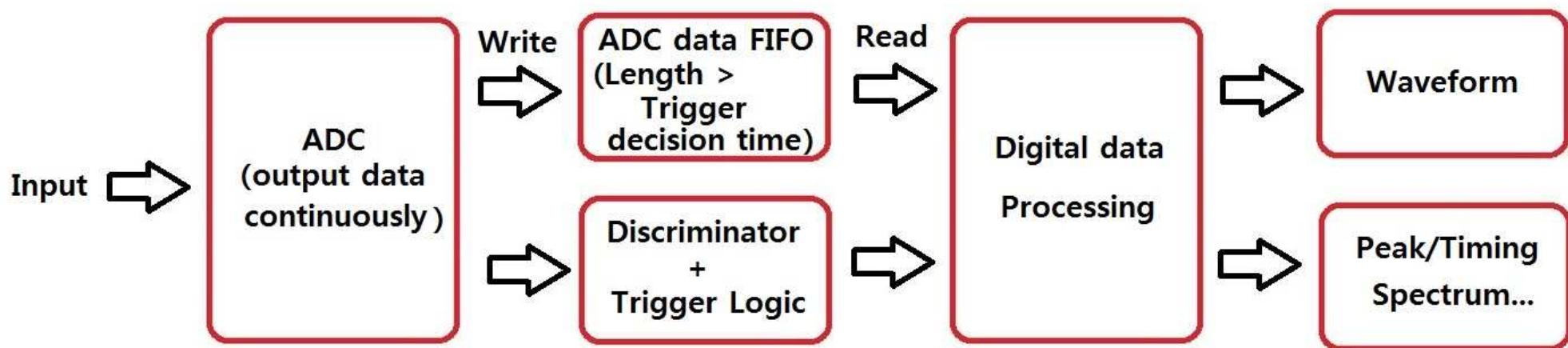
# Structure of typical Flash ADC board



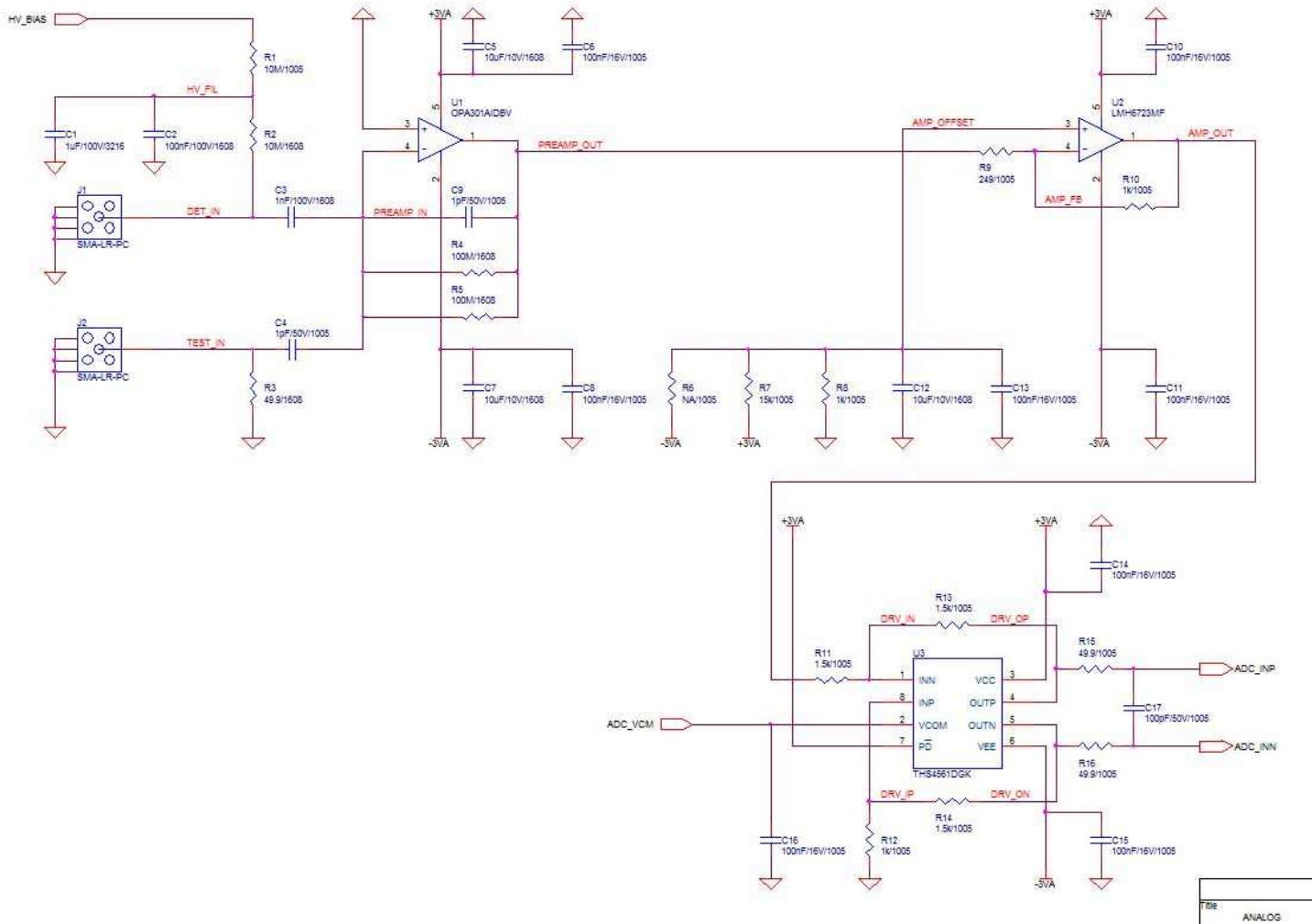
# Structure of simpler Flash ADC board



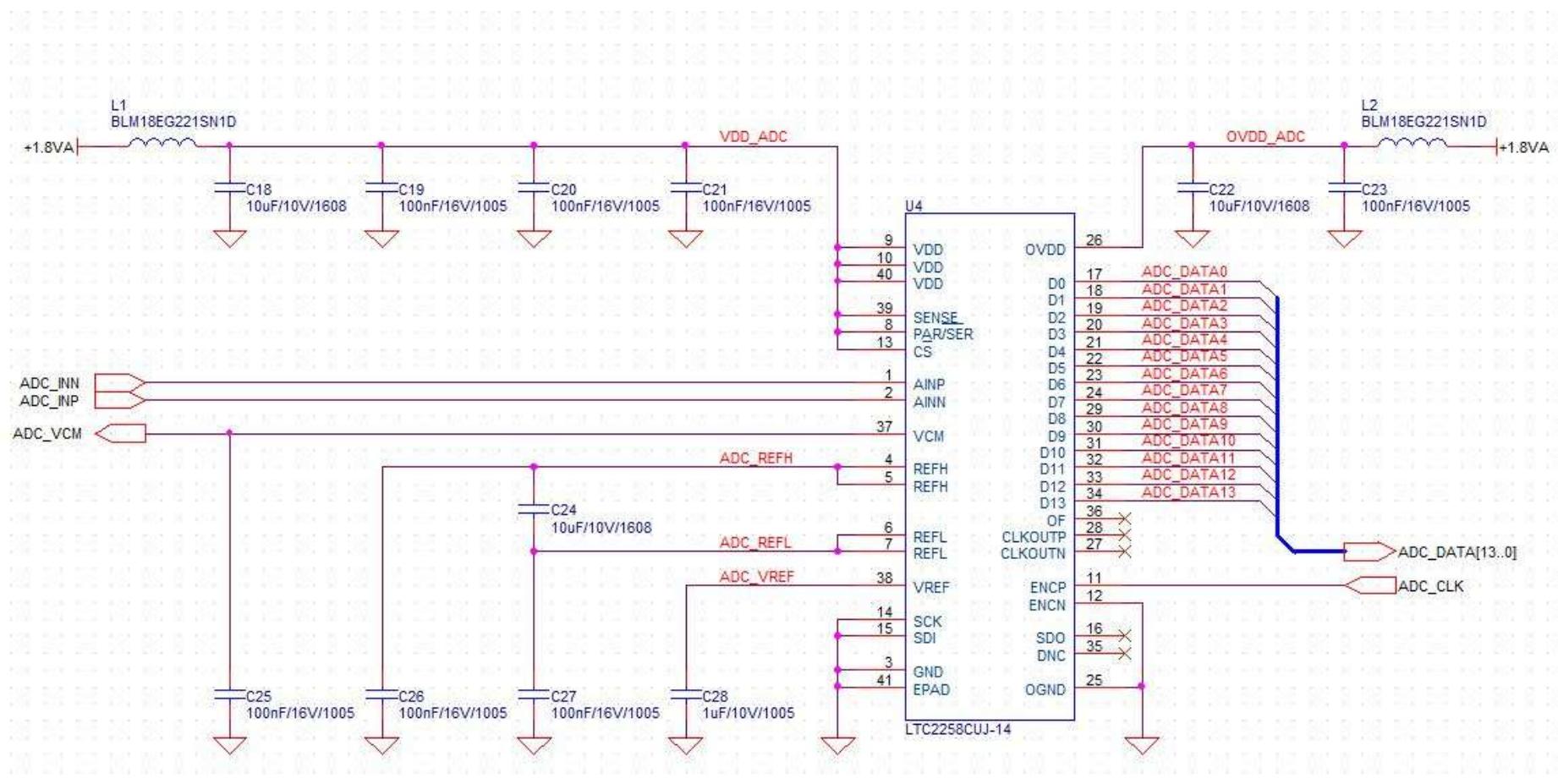
# Data processing in Flash ADC board



# Flash ADC board analog circuits example



# Flash ADC board ADC circuits example



# Choosing FPGA(Field Programmable Gate Array)

Table 1: 7 Series Families Comparison

Maximum Capability	Artix-7 Family	Kintex-7 Family	Virtex-7 Family
Logic Cells	215K	478K	1,955K
Block RAM <sup>(1)</sup>	16 Mb	34 Mb	68 Mb
DSP Slices	740	1,920	3,600
Peak DSP Performance <sup>(2)</sup>	929 GMAC/s	2,845 GMAC/s	5,335 GMAC/s
Transceivers	16	32	96
Peak Transceiver Speed	6.6 Gb/s	12.5 Gb/s	28.05 Gb/s
Peak Serial Bandwidth (Full Duplex)	211 Gb/s	800 Gb/s	2,784 Gb/s
PCIe Interface	x4 Gen2	x8 Gen2	x8 Gen3
Memory Interface	1,066 Mb/s	1,866 Mb/s	1,866 Mb/s
I/O Pins	500	500	1,200
I/O Voltage	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V	1.2V, 1.35V, 1.5V, 1.8V, 2.5V, 3.3V
Package Options	Low-Cost, Wire-Bond, Lidless Flip-Chip	Low-Cost, Lidless Flip-Chip and High-Performance Flip-Chip	Highest Performance Flip-Chip

Table 5: Kintex-7 FPGA Feature Summary by Device

Device	Logic Cells	Configurable Logic Blocks (CLBs)		DSP Slices <sup>(2)</sup>	Block RAM Blocks <sup>(3)</sup>			CMTs <sup>(4)</sup>	PCIe <sup>(5)</sup>	GTx	XADC Blocks	Total I/O Banks <sup>(6)</sup>	Max User I/O <sup>(7)</sup>
		Slices <sup>(1)</sup>	Max Distributed RAM (Kb)		18 Kb	36 Kb	Max (Kb)						
XC7K70T	65,600	10,250	838	240	270	135	4,860	6	1	8	1	6	300
XC7K160T	162,240	25,350	2,188	600	650	325	11,700	8	1	8	1	8	400
XC7K325T	326,080	50,950	4,000	840	890	445	16,020	10	1	16	1	10	500
XC7K355T	356,160	55,650	5,088	1,440	1,430	715	25,740	6	1	24	1	6	300
XC7K410T	406,720	63,550	5,663	1,540	1,590	795	28,620	10	1	16	1	10	500
XC7K420T	416,960	65,150	5,938	1,680	1,670	835	30,060	8	1	32	1	8	400
XC7K480T	477,760	74,650	6,788	1,920	1,910	955	34,380	8	1	32	1	8	400

Table 6: Kintex-7 FPGA Device-Package Combinations and Maximum I/Os

Package <sup>(1)</sup>	FBG484		FBG676 <sup>(2)</sup>		FFG676 <sup>(2)</sup>		FBG900 <sup>(3)</sup>		FFG900 <sup>(3)</sup>		FFG901		FFG1156			
	Size (mm)	23 x 23		27 x 27		27 x 27		31 x 31		31 x 31		31 x 31		35 x 35		
		1.0		1.0		1.0		1.0		1.0		1.0		1.0		
Device	GTx	I/O		GTx	I/O		GTx	I/O		GTx	I/O		GTx	I/O		
		HR <sup>(4)</sup>	HP <sup>(5)</sup>		HR <sup>(4)</sup>	HP <sup>(5)</sup>		HR <sup>(4)</sup>	HP <sup>(5)</sup>		HR <sup>(4)</sup>	HP <sup>(5)</sup>	GTx	HR <sup>(4)</sup>	HP <sup>(5)</sup>	
XC7K70T	4	185	100	8	200	100										
XC7K160T	4	185	100	8	250	150	8	250	150							
XC7K325T				8	250	150	16	350	150	16	350	150		24	300	0
XC7K355T				8	250	150	16	350	150	16	350	150				
XC7K410T				8	250	150	8	250	150	16	350	150				
XC7K420T														28	380	0
XC7K480T														28	380	0