

D_RD_27: Study of modern FPGA device and associated new technology, and search for possible application in High Energy experiments

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on behalf of the D_RD_27 group

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2024 Joint Workshop of FKPPN and TYL/FJPPN

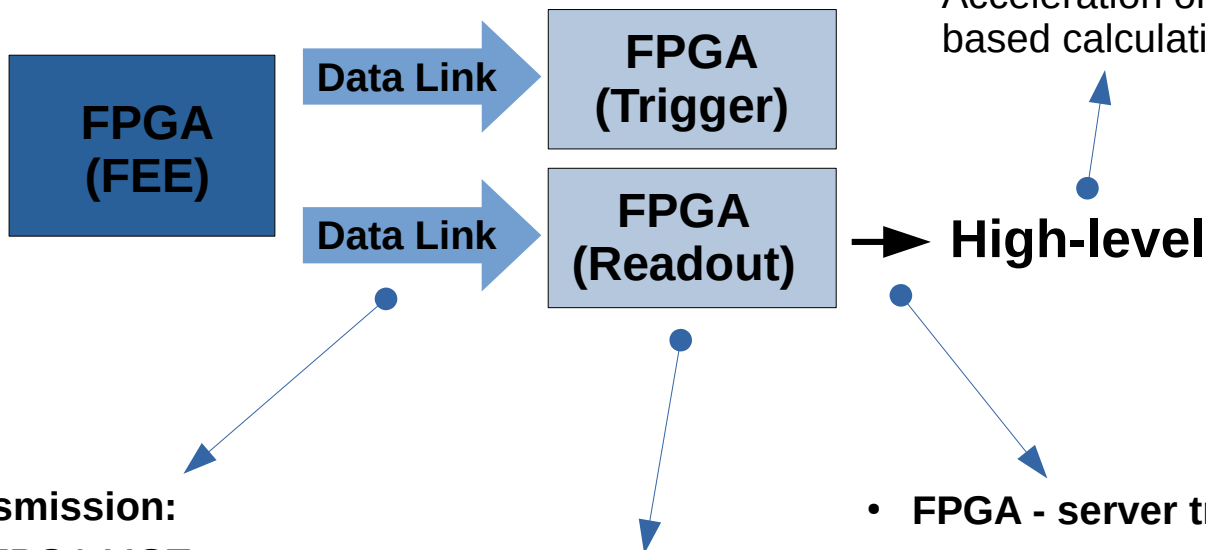
@ KISTI

23rd May, 2024



Application of FPGA in HEP experiments

- **Our target:** Study the latest COTS FPGA devices and their associated new technologies for possible application and upgrade in different aspects of HEP experiments.



- **Hardware acceleration:**
 - Not only CPU, but also GPU and FPGA.
 - Acceleration on software-based calculation.

- **FPGA - FPGA transmission:**

- Optical link with FPGA MGT and optical modules.
- Non-Return-to-Zero (NRZ).
- Different encoding based on protocol design purposes. e.g. 8B/10B and 64B/66B.
 - <10 Gbps for DAQ.
 - <25 Gbps for TRG.

- Strong **FPGA devices** with:

- Larger number of cells.
- Larger data bandwidth.

are critical for the usage in:


- **TRG:** complicated algorithm implementation.
- **DAQ:** collect and process large data.

- **FPGA - server transmission:**

- Data transmission and system slow control.
- GbE, PCI-express, VME, etc.
- PCI-Express is the most popular one nowadays: PCIe40 in ALICE, LHCb, and Belle II.

Versal project

- Our project is mainly based on the Xilinx Versal series of ACAP.
- KEK together with Japanese HEP community purchased a few evaluation kits.
 - Plan: Common and general studies on the new technologies for future electronics device's R&D. Now we plan to use Versal for L1 TRG, DAQ or HLT purpose.
- The features of different Versal series ACAP:
 - AI engine: convenient interface to implement ML core into firmware.
 - High Bandwidth Memory (HBM).
 - Larger number of cells + High transmission bandwidth.



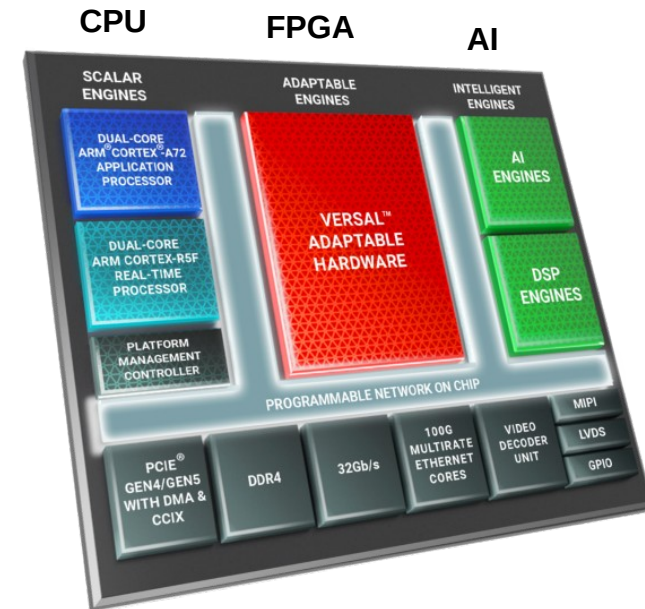
HBM Series
Recently announced, features hyper integration of fast memory, secure data, and adaptive compute for memory bound, compute intensive, high bandwidth applications.
[View HBM Series >](#)

AI Core Series
Delivers breakthrough AI inference and wireless acceleration with AI Engines that deliver over 100X greater compute performance than today's server-class CPUs.

AI Edge Series
Delivers over 4X AI performance/watt vs. leading GPUs for power- and thermally-constrained edge applications, accelerating the whole application from sensor to AI to real-time control.

Prime Series
The foundational Versal® ACAP series, providing a wide range of devices with broad applicability across multiple markets.
[View Prime Series >](#)

Premium Series
Breakthrough integration of networked, power-optimized cores on an adaptable platform for the most challenging compute and networking applications.



source: Xilinx website

Versal project: General plan, roadmap, and collaboration

- Our goal: R&D of a new general FPGA device using the Versal ACAP.
 - A L1 TRG, DAQ, or HLT device, and also general for different experiments.
 - One clear target is **UT5 for L1 TRG of both Belle II and ATLAS**.

1st year:

- Study the properties of the fundamental functionalities with the kits:
 - GTM (PAM4), PCIe Gen5, AI engine, DPU, etc.
- Prepare basic application for each of them for other members.

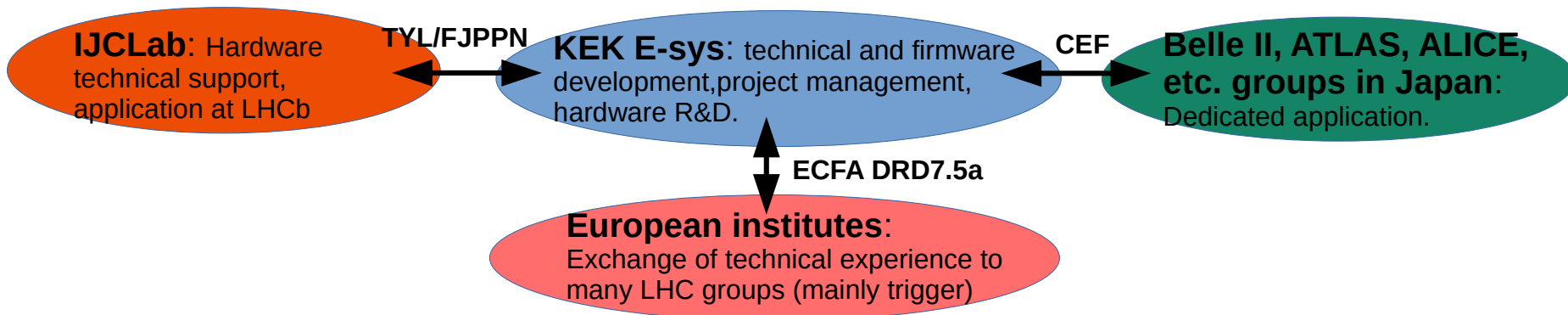
Here we are now with VPK120 and VCK190. →

2nd year:

- Make general transmission protocols for GTM (PAM4), PCIe Gen5, and do performance study.
- Implement various Trigger algorithms (Belle II, ATLAS, etc).
- Connect to existing systems to take real-time data and check performance.

3rd year:

- Future universal device: L1 TRG, DAQ readout, or HLT.
 - Discussion.
 - Schematic/PCB design for the prototype boards.
 - Test with experiments people.



D_RD_27 members

- Activities in 2023:
 - Japan → France: Visited IJCLab for discussion on progress and future collaboration with CPPM Marseille for joint study on PCIe related R&D.
 - France → Japan: Participated the Belle II general meeting for PCIe40 work.
- New members in 2024 application:
 - KEK ACCL: High-speed ADC system with WhiteRabbit using PCIe DMA readout.
 - CPPM Marseille: PCIe400 readout upgrade.

France			Japan		
Name	Institute		Name	Institute	
<u>Daniel Charlet</u>	IJCLab Orsay	PCIe readout device for Belle II / LHCb	<u>Yun-Tsung Lai</u>	KEK IPNS	E-sys, Belle II
Patrick Robbe			Manobu Tanaka		E-sys
Tak-Shun Lau			Makoto Tomoto		ATLAS
Emi Kou			Satoru Yamada		Belle II
			Yutaka Ushiroda		Belle II
			Kunihiro Nagano		ATLAS
			Taichiro Koga		Belle II
			Yu Nakazawa		Belle II

New members

Julien Langouet	CPPM Marseille	PCIe400 readout upgrade	Hiroshi Kaji	KEK ACCL	SuperKEKB
Paul Bibron					
Renaud Le Gac					

- Progress so far:
 - Study on fundamental elements.

PAM4

- Tested with QSFPDD.
- Customized protocol.

PCIe

- Tested with PCIe-CPM.
- Event readout and exchange logic.
- Belle II PCIe40

AI engine

- Design flow.
- Tested with many algorithms.

DPU

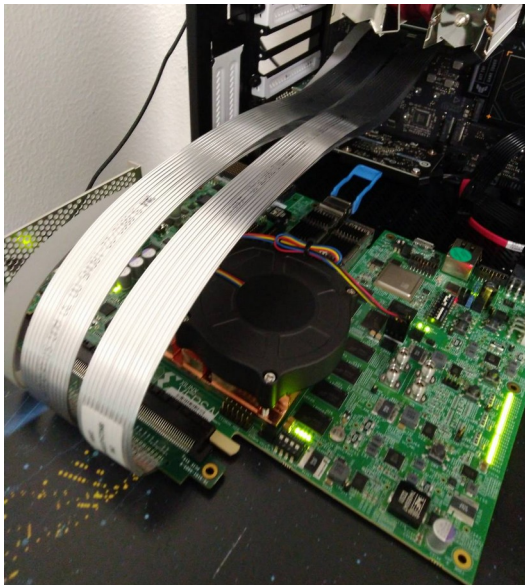
- Working environment with VCK190.
- GPU quantization.
- Tested with different algorithms.

Test bench setup @ KEK E-sys group

- The test bench of VPK120 has been built at E-sys group and released to our members for dedicated studies.
- VCK190 has also arrived at KEK in March. Preparation study is ongoing and will be ready soon.
- Special thanks to Mathis Maurice, internship in E-sys group in 2023 summer, for helping this VPK120 preparation work!



PC side: PCIe Gen5 x16 slot



VPK120 test bench: 2023 summer

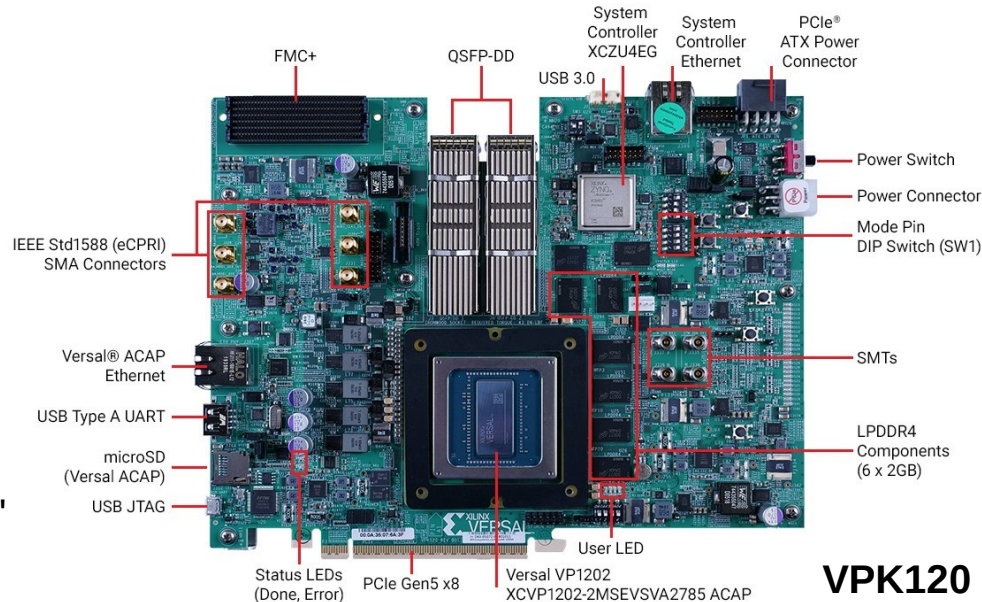
PC side: PCIe Gen4 x8 slot



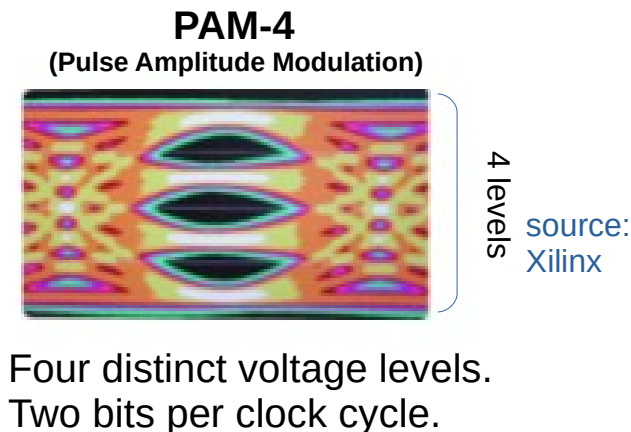
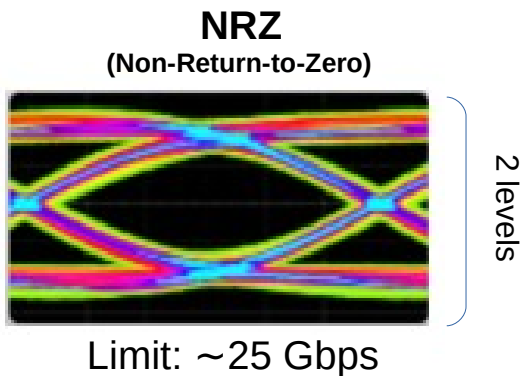
VCK190 test bench: 2024 March

Data transmission with VPK120

- GTYP: PCIe 5.0 (16) and FMC+ (8)
 - 1.25 ~ 32.75 Gb/s.
 - Various encoder supported.
- GTM: QSFPDD (8*2)
 - NRZ:
 - 9.5 ~ 15, 19 ~ 29 Gb/s.
 - PAM4:
 - 19 ~ 30, 38 ~ 60 Gb/s
 - 76 ~ 112 Gb/s: "Half density mode" by combining two lanes.
 - No encoding is supported. Need to be make them manually in RTL.



VPK120

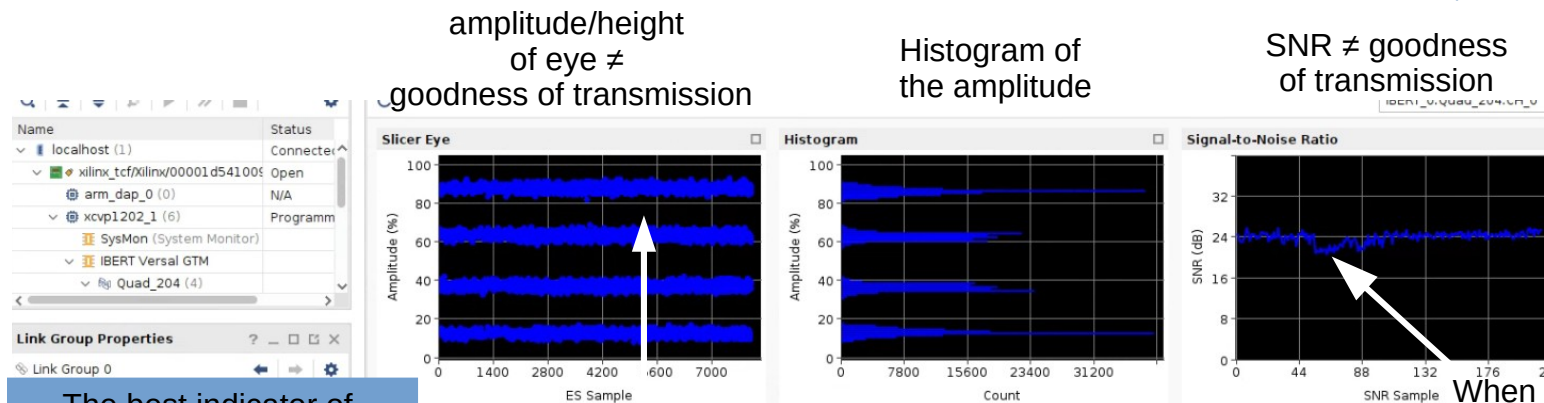


PAM4 56 Gbps with GTM, QSFPDD loopback

- PAM4, 56 Gbps per lane. QSFPDD loopback module.
- Parameter tuning on cursor position and termination voltage, etc, is necessary to have stable transmission (0 bit error).



DesignCon 2019 Enabling IBIS-AMI Simulations for Systems Containing PAM4 Retimers at 112Gbps



The best indicator of goodness of transmission: **0 error (BER)**

A good set of parameters

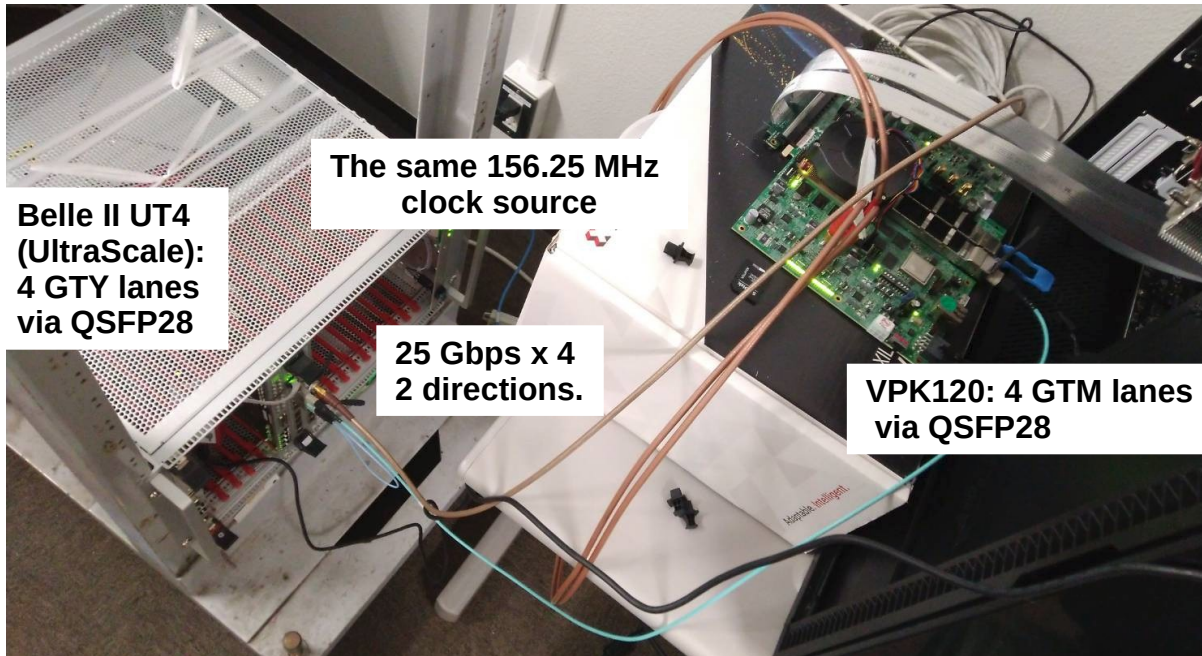
When parameters were under tuning.

Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	TX Pre-Cursor	TX Pre-Cursor2	TX Post-Cursor	TX Main-Cursor	Inject Error	TX Reset	RX Reset
				Reset	PRBS 31	PRBS 31	0 dB	0 dB	0 dB	0.502 Vdd	Inject	Reset	Reset
56.414 Gbps	3.2148E11	0E0	3.003E-12	Reset	PRBS 31	PRBS 31	0 dB	0 dB	0 dB	0.502 Vdd	Inject	Reset	Reset
56.414 Gbps	2.7378E11	0E0	3.556E-12	Reset	PRBS 31	PRBS 31	0 dB	0 dB	0 dB	0.502 Vdd	Inject	Reset	Reset
56.402 Gbps	1.8918E11	0E0	6.095E-12	Reset	PRBS 31	PRBS 31	0 dB	0 dB	0 dB	0.502 Vdd	Inject	Reset	Reset
56.402 Gbps	1.2028E11	0E0	1.143E-11	Reset	PRBS 31	PRBS 31	0 dB	0 dB	0 dB	0.502 Vdd	Inject	Reset	Reset

Protocol development and connection test

- Both 8B/10B and 64B/66B (sync. gearbox) are tested with GTM.
- Raw mode with No encoding: A new generalized protocol has been also made.
 - Similar logic to my Belle II TRG protocol design.
 - (de)scrambler for DC balance.
 - Tested to be stable for both NRZ and PAM4.
- Using this new generalized protocol, connection test (25 Gbps x4, NRZ) between Belle II UT4 and VPK120 has been also tested. Stable in few hours.

Belle II UT4



**Belle II UT4
(UltraScale):
4 GTY lanes
via QSFP28**

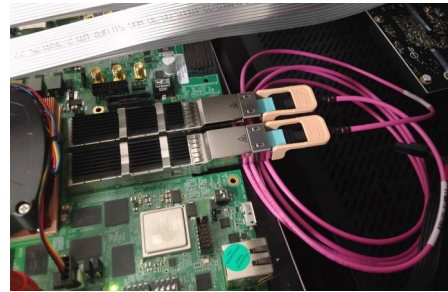
**The same 156.25 MHz
clock source**

**25 Gbps x 4
2 directions.**

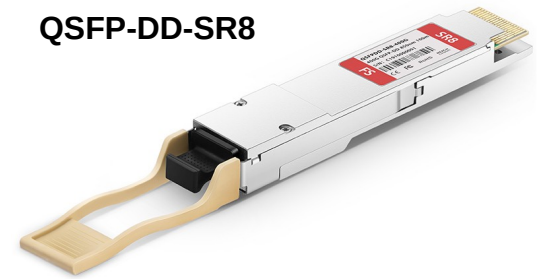
**VPK120: 4 GTM lanes
via QSFP28**

Transmission test with PAM4 and QSFPDD

- Using the same transmission protocol, we have also successfully tested the real transmission:
 - QSFPDD-SR8 with MPO16.
 - 53.125 Gb/s x 16 lanes.
 - Only this line rate is supported.

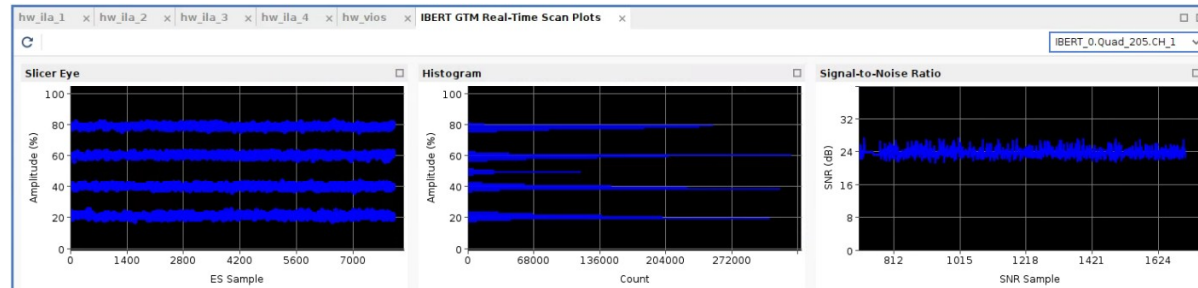


QSFP-DD-SR8

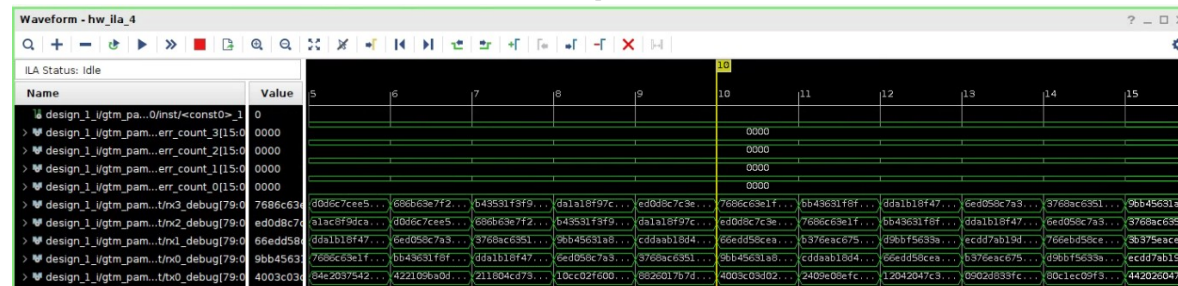


- BERT in 3 days:
 - Our self-designed protocol.
 - PRBS16 patterns.
 - BER of the worst lane: 9.0×10^{-14}
 - Combined BER: 6.7×10^{-15}

- Latency:
 - 60~70 clocks in 332 MHz.
 - 180~210 ns.



PRBS16 patterns



PCIe-CPM test with Versal kits

- CPM-PCIe example from Xilinx: XTP712
 - CPM: building block design for PCIe with integrating DMA, CIPS, NOC, etc.
 - PCIe Gen4 x8: GTYP links are up. 16 Gbps per lane.
- Driver software: QDMA, also a Xilinx IP.

Hardware

Name	Status
Quad_102 (4)	
R0_CH_0	15.987 Gbps
R0_CH_1	15.977 Gbps
R0_CH_2	15.97 Gbps
R0_CH_3	15.954 Gbps
Quad_103 (4)	
R0_CH_0	15.073 Gbps
R0_CH_1	15.063 Gbps
R0_CH_2	15.08 Gbps
R0_CH_3	15.084 Gbps
DDRM_C_1 (LPDDR4) (x1y0)	PASS
DDRM_C_2 (LPDDR4) (x1y0)	PASS
DDRM_C_3	DISABLED

Properties

Select an object to see properties

DDRMC - DDRMC_1 **DDRMC - DDRMC_2**

Status

Name: DDRMC_2

Calibration Status: **PASS**

DDRMC Status: **GOOD**

Gate Tracking Status: **Running**

Message: No errors detected during calibration.

Error:

Calibration

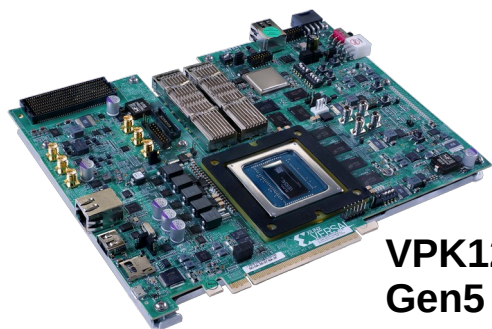
Stage	Status
CAL_STAGE.01_F0_PHY_BISC	Pass
CAL_STAGE.02_F0_MEM_INIT	Pass
CAL_STAGE.03_F0_LPDDR4_CS_CA_TRAIN	Pass
CAL_STAGE.04_F0_DQS_GATE_CAL	Pass
CAL_STAGE.05_F0_WRITE_LEVELING	Pass
CAL_STAGE.06_F0_READ_DQ_CAL	Pass
CAL_STAGE.07_F0_WRITE_DQ_CAL	Pass

Margins Analysis

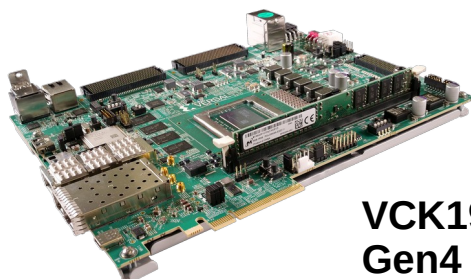
Name	Left Margin (taps)	Center Point (taps)
Byte 0		
Nibble 0		61
Nibble 1		61
Byte 1		
Nibble 0		62
Nibble 1		62
Byte 2		
Nibble 0		62
Nibble 1		62
Byte 3		
Nibble 0		61
Nibble 1		60
Byte 4		
Nibble 0		64
Nibble 1		64

Tcl Console Messages Serial I/O Links Serial I/O Scans

ig	DPE Enabled	Inject Error	TX Reset	RX Reset	RX PLL Status	TX PLL Status	Loopback Mode	Termination Voltage	RX Common Mode	TXUSERCLK Freq	RXUSERCLK Freq	T
n	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked	User Design	800mv	Programmable	499.512	499.292	U
n	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked	User Design	800mv	Programmable	499.512	499.292	U
n	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked	User Design	800mv	Programmable	499.072	498.779	U
n	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked	User Design	800mv	Programmable	499.292	499.438	U
n	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked	User Design	800mv	Programmable	498.413	499.365	U
n	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked	User Design	800mv	Programmable	498.413	499.585	U
n	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked	User Design	800mv	Programmable	498.486	498.560	U
n	<input checked="" type="checkbox"/>	Inject	Reset	Reset	Locked	Locked	User Design	800mv	Programmable	498.560	499.512	U



VPK120
Gen5 x 16

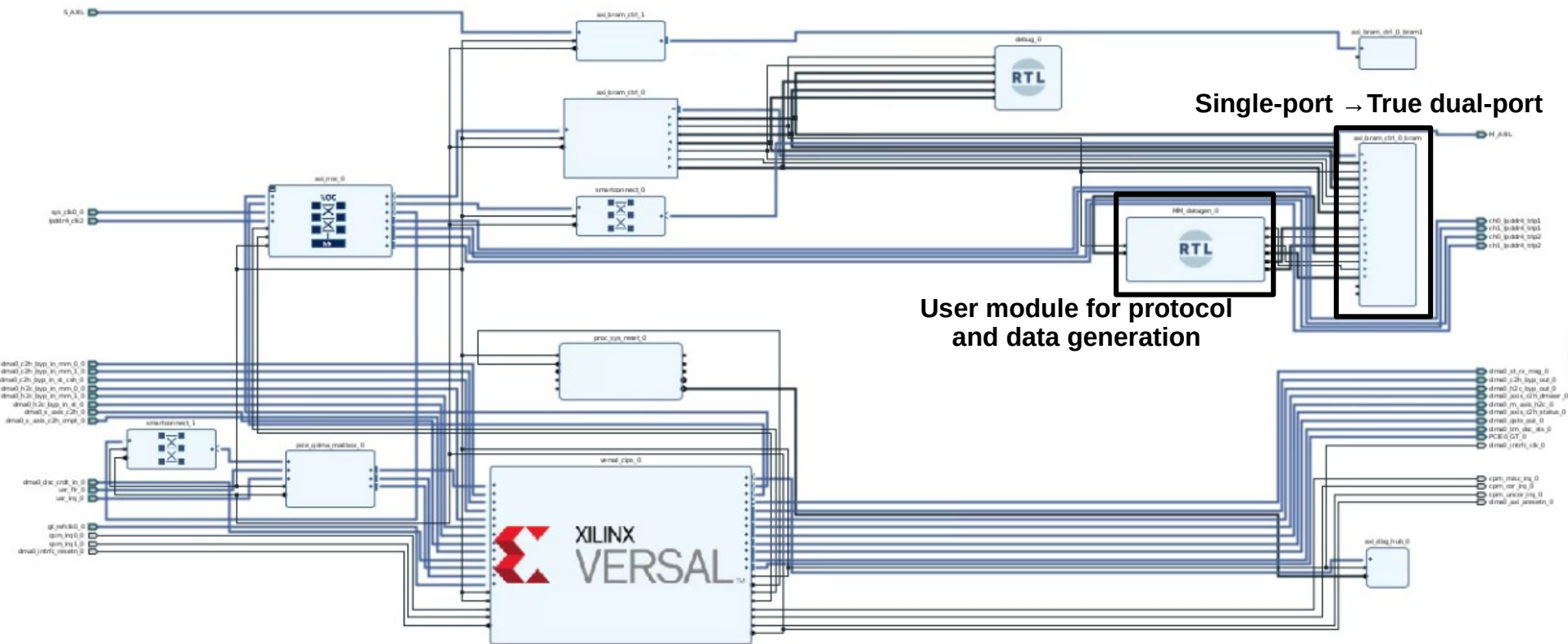


VCK190
Gen4 x 8

```
[root@cef01 linux-kernel]# ./bin/dma-ctl dev list
qdma02000      0000:02:00.0    max QP: 8, 0~7
qdma02001      0000:02:00.1    max QP: 0, --
qdma02002      0000:02:00.2    max QP: 0, --
qdma02003      0000:02:00.3    max QP: 0, --
[root@cef01 linux-kernel]# ./bin/dma-ctl qdma02000 q add idx 0 dir bi
dma-ctl: Warn: Default mode set to 'mm'
qdma02000-MM-0 H2C added.
qdma02000-MM-0 C2H added.
Added 1 Queues.
[root@cef01 linux-kernel]# ./bin/dma-ctl qdma02000 q start idx 0 dir bi
dma-ctl: Info: Default ring size set to 2048
1 Queues started, idx 0 ~ 0.
1 Queues started, idx 0 ~ 0.
[root@cef01 linux-kernel]# ./bin/dma-to-device -d /dev/qdma02000-MM-0 -s 32
size=32 Average BW = 177.37688 KB/sec
[root@cef01 linux-kernel]# ./bin/dma-from-device -d /dev/qdma02000-MM-0 -s 32
size=32 Average BW = 132.445391 KB/sec
[root@cef01 linux-kernel]# ./bin/dma-ctl qdma02000 q stop idx 0 dir bi
Stopped Queues 0 -> 0.
[root@cef01 linux-kernel]# ./bin/dma-ctl qdma02000 q del idx 0 dir bi
Deleted Queues 0 -> 0.
```


PCIe-CPM firmware: Event readout using MM mode

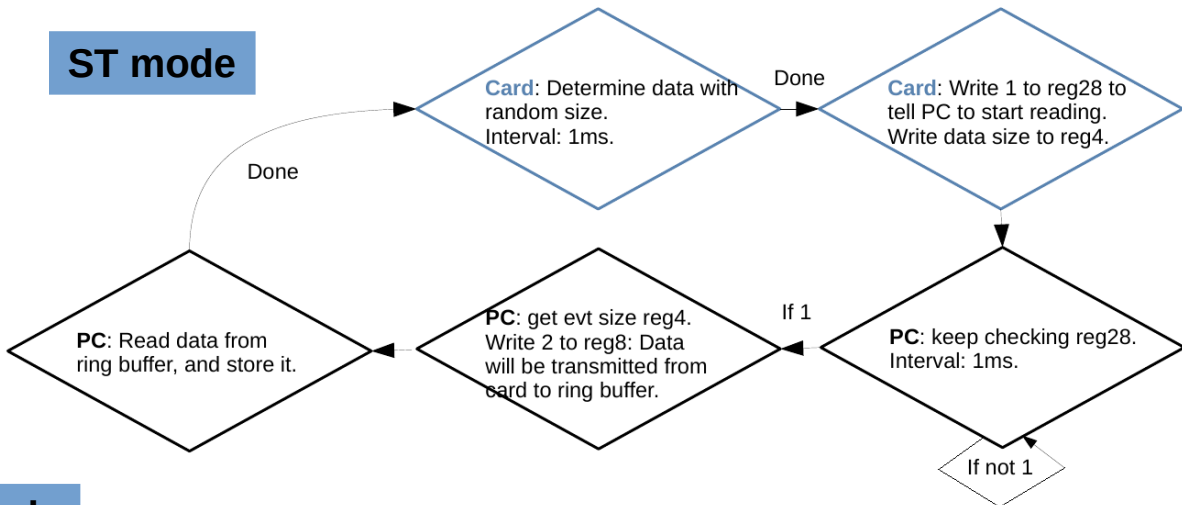
- New firmware based on MM mode.



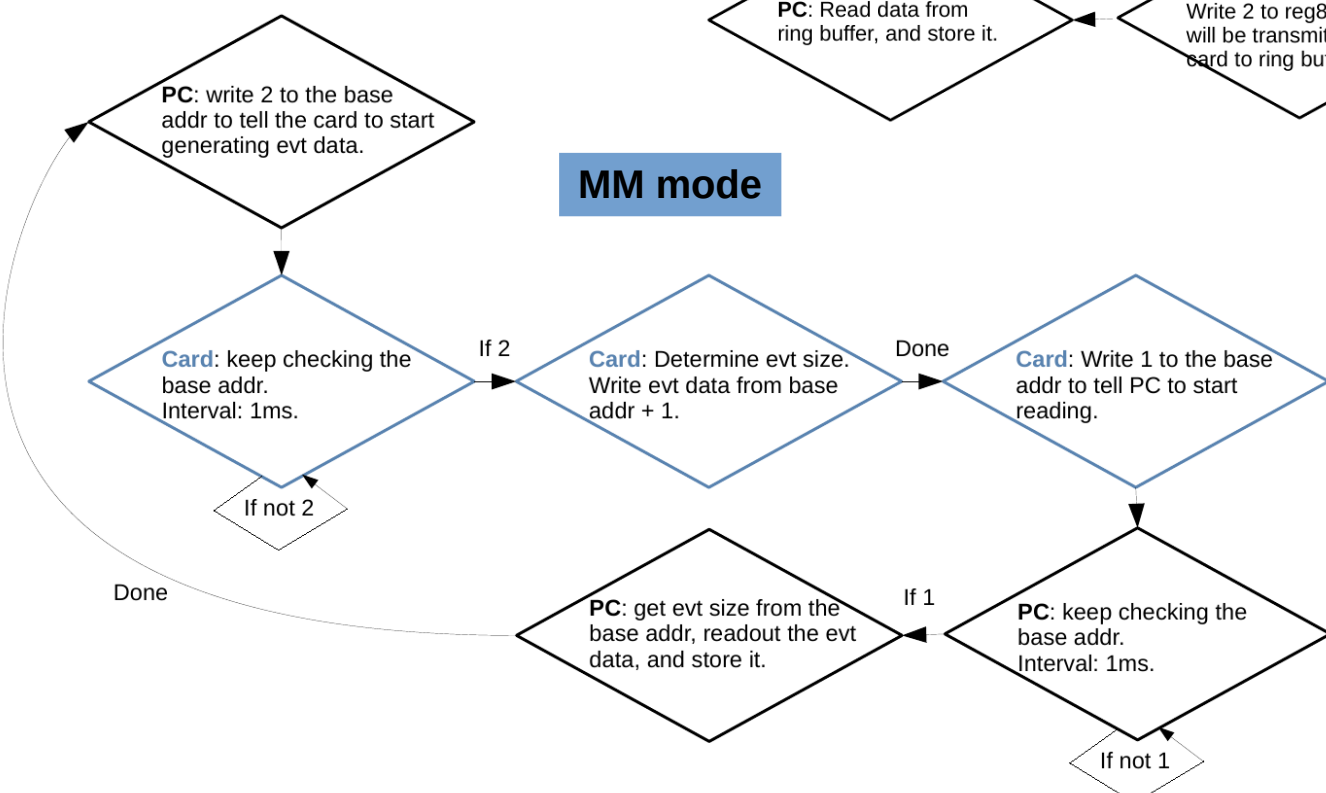
PCIe-CPM firmware: Event readout

- State machine of the readout protocol between PC and FPGA:
- Not fully optimized yet:
 - Long waiting time.

ST mode



MM mode



PCIe-CPM firmware: Event readout (cont'd)

- Test:
 - Working correctly with random size.

```
root@cef01:/home/ytlai/versal/dma_ip_drivers-master_202311/QDMA/linux-kernel/apps/user-readout# ./user-readout d /dev/qdma02000-MM
-2 -c 10
host buffer 0x1008, 0x5558ab141000.
evt filled
1 192 0 64
evt size:384 bytes
evt taking done
waiting...
waiting...
waiting...
evt filled
3 128 0 64
evt size:832 bytes
evt taking done
waiting...
waiting...
waiting...
waiting...
evt filled
Workspace Switcher
evt size:256 bytes
evt taking done
waiting...
waiting...
waiting...
waiting...
evt filled
3 0 0 64
evt size:704 bytes
evt taking done
waiting...
```

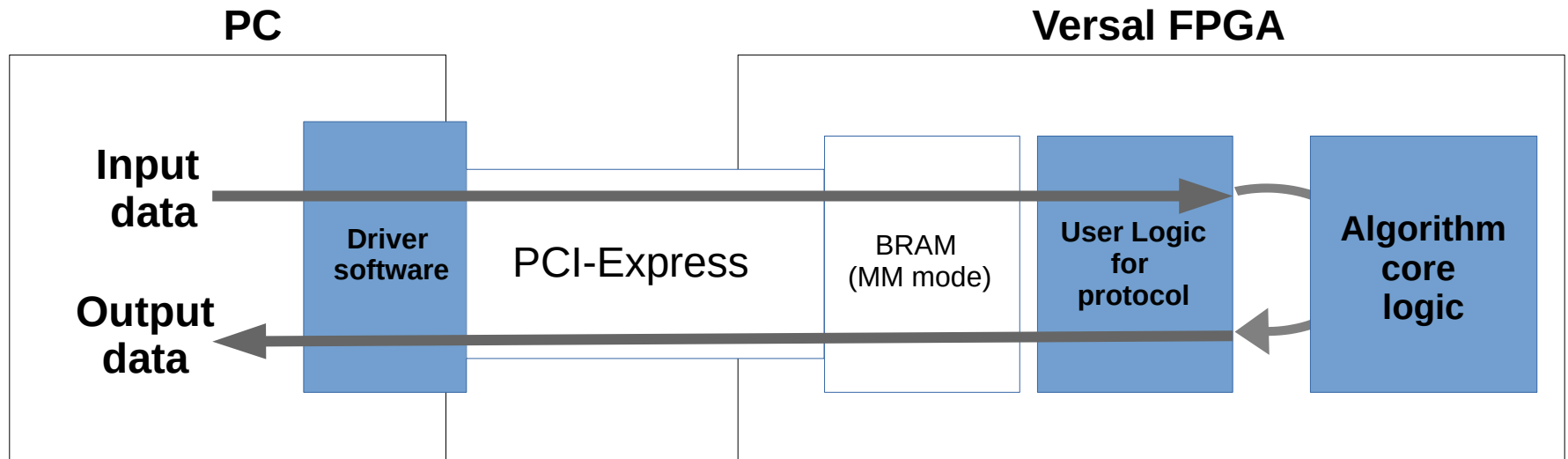
Manual readout software

Store event data with random size

```
512 3月 5 11:01 0.log
192 3月 5 11:01 10.log
512 3月 5 11:01 11.log
448 3月 5 11:01 12.log
384 3月 5 11:01 13.log
128 3月 5 11:01 14.log
0 3月 5 11:01 15.log
0 3月 5 11:01 16.log
0 3月 5 11:01 17.log
576 3月 5 11:01 18.log
512 3月 5 11:01 19.log
448 3月 5 11:01 1.log
448 3月 5 11:01 20.log
384 3月 5 11:01 21.log
320 3月 5 11:01 22.log
0 3月 5 11:01 23.log
576 3月 5 11:01 24.log
512 3月 5 11:01 25.log
448 3月 5 11:01 26.log
128 3月 5 11:01 27.log
64 3月 5 11:01 28.log
0 3月 5 11:01 29.log
384 3月 5 11:01 2.log
0 3月 5 11:01 30.log
576 3月 5 11:01 31.log
```

PCIe-CPM firmware: Event exchange

- A data exchange flow is also made for firmware and software.
 - For both MM and ST modes.
- 1 event in - 1 event out.
- In order to test the algorithm core logic to be implemented in Versal kits.



PCIe40 upgrade at Belle II

- PCIe40 upgrade and its commissioning at Belle II has been complete in 2023.
 - KEK and IJCLab keeps working on the improvement.
 - Still important reference for new system R&D.
- Double PCIe bandwidth: 8 lanes → 16 lanes.
 - Both firmware and driver software for DMA are modified.
 - Improved throughput
 - Internal data generator: 14 GB/s.
 - Pseudo FEE, 32 channels at 27 kHz: 7.3 GB/s

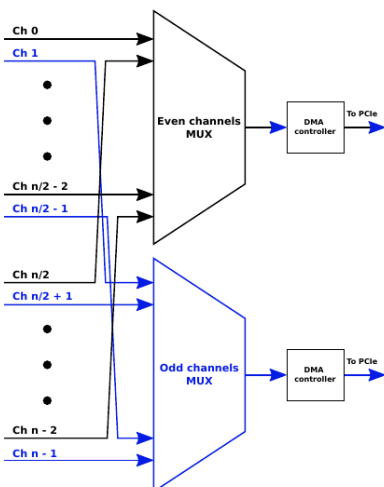
PCIe40: PCIe Gen3 x 16



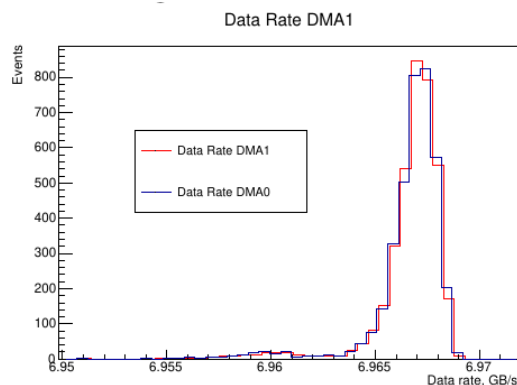
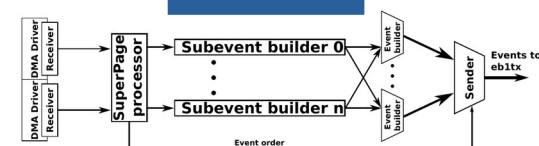
Study by Dmytro Levit (KEK) and Tak-Shu Lau (IJCLab)

- Interface to Belle II Trigger&Timing system "b2tt":
 - From RJ45 to Opt link.
 - Better stability in operation.
 - Modification on PCIe40 circuit needed.

Firmware



Software



AI engine

- Design flow with Vivado/Vitis:
 - C++ programmable design for AI engine.
 - Integrated in PL design.
- Our group will prepare a manual and tutorial for using AI engine for experimental groups' algorithms development.

Vivado

- Open an **example project** for VCK190:
 - Versal Extensible Embedded system with AI engine.
- Export **platform**

.xsa file

taking this file

Vitis

Workspace

Platform

AI engine component

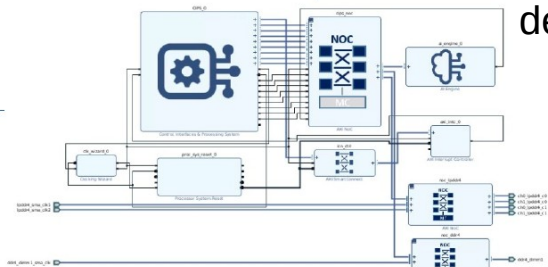
From example. src, kernel and data.
Algorithm is defined here.

HLS Component: mm2s
with mm2s.cpp

HLS Component: s2mm
with s2mm.cpp

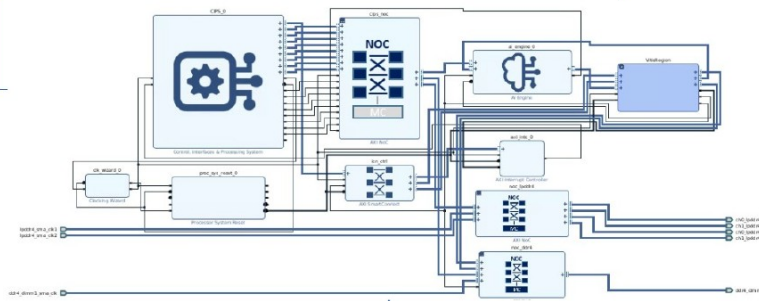
System project Component
for integration

```
> base_pfm_vck190 [Platform]
> mm2s [HLS]
> s2mm [HLS]
> simple_ale_application [AI Engine]
> simple_ale_application_system_project
```



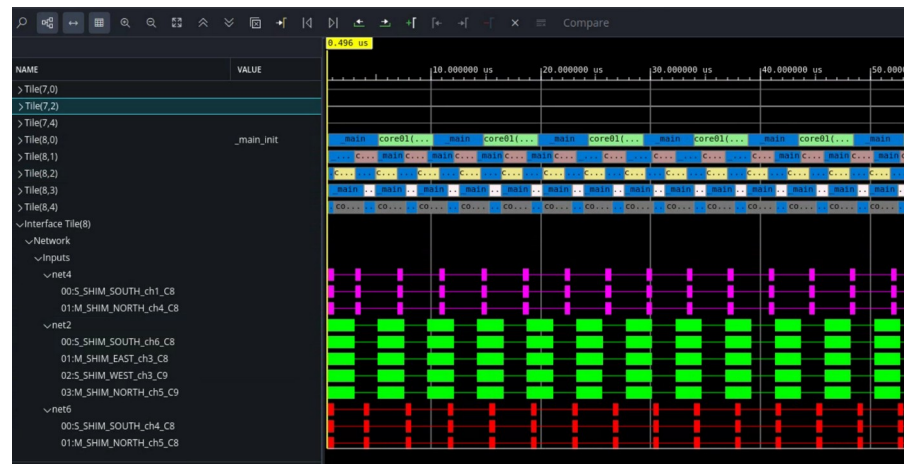
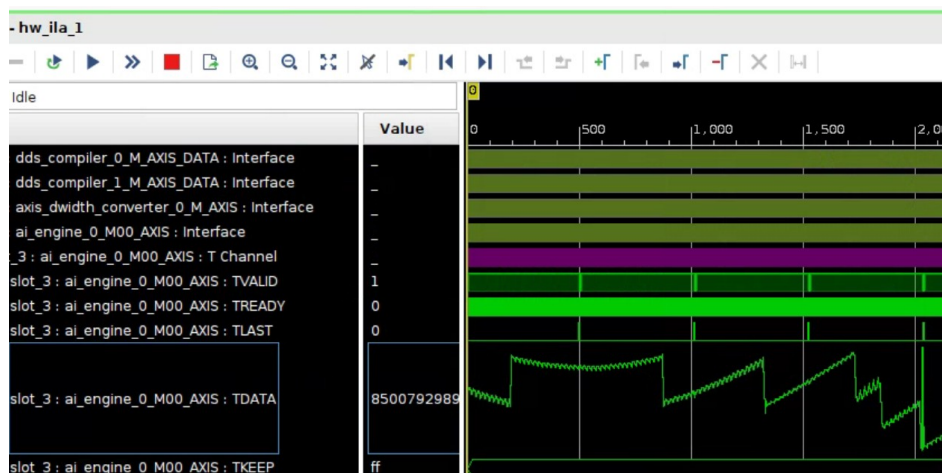
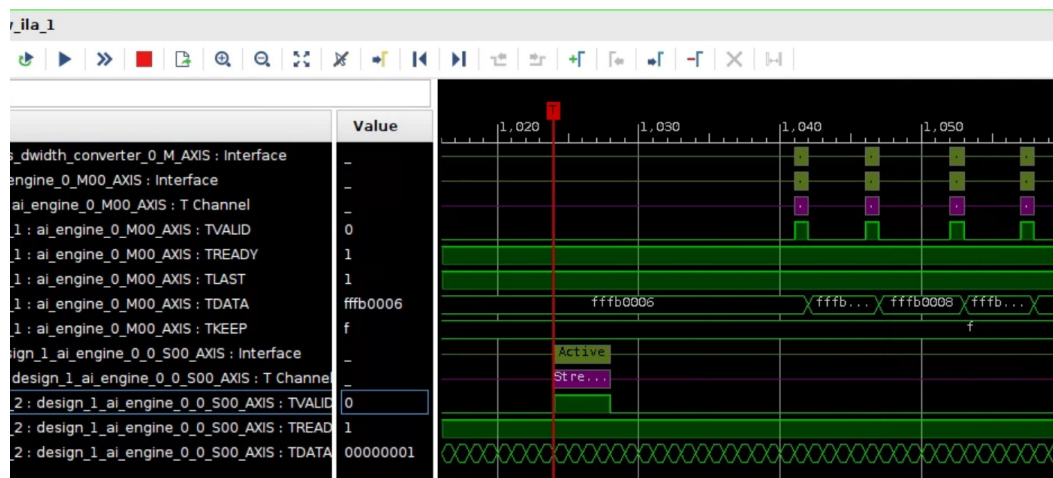
Vivado

Get the final **firmware project**
With AI engine, mm2s, s2mm to NOC



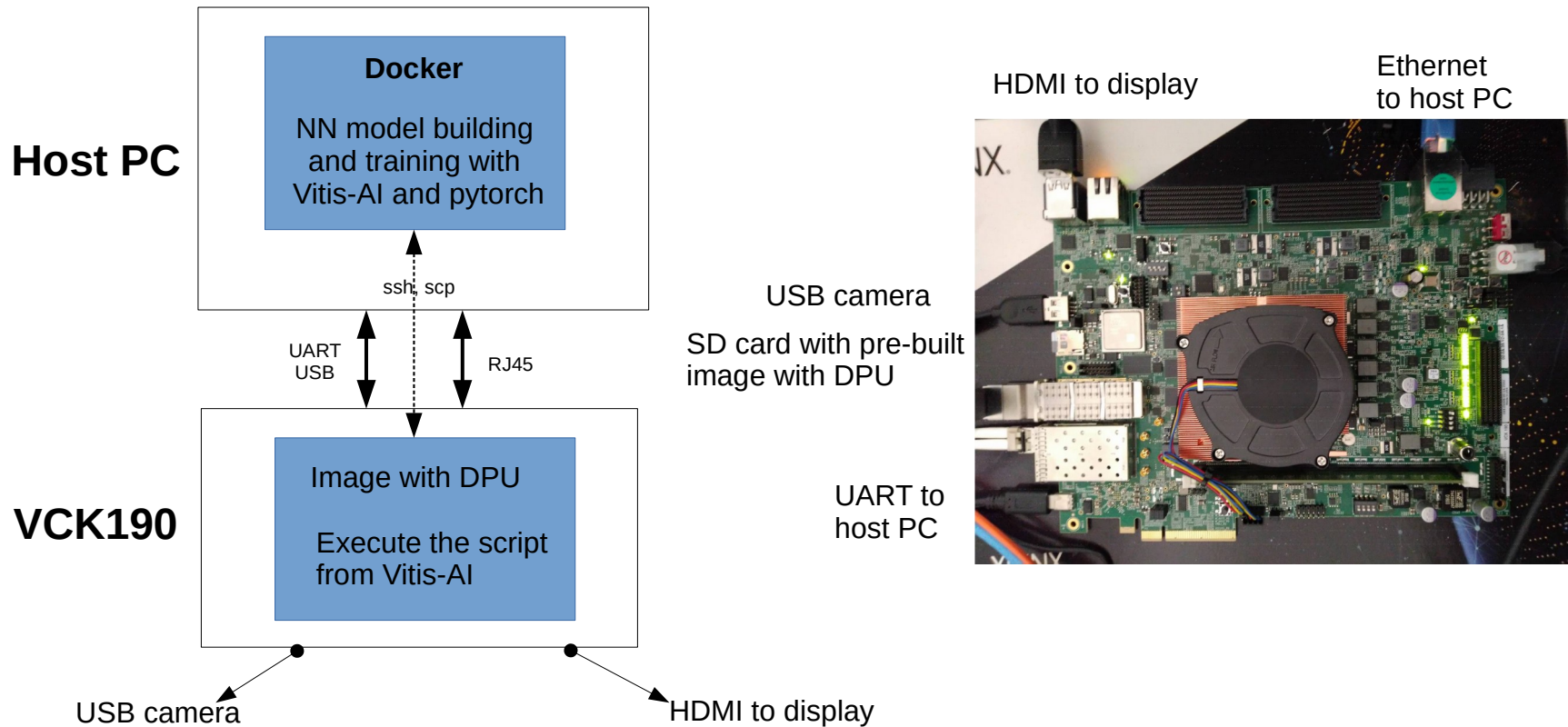
AI engine: test

- The work flow of building up a firmware with AI engine has been studied.
 - PL → AI engine → PL.
- Some logics were tested.
 - Arithmetic calculation
 - FIR filter
 - leNet



Vitis-AI with DPU

- VCK190 has another feature of Deep Learning Processor Unit (DPU), which is a configurable computation engine dedicated to convolutional neural networks.
- The design flow does not involve Vivado for PL design. The device is utilized with a small operation system like a server, and works can be executed in it.
 - A higher-level application.



Vitis-AI with DPU: test

- The environment with docker and DPU setup for VCK190 has been ready.
 - GPU quantization.
 - Image and video processing.
 - ATLAS top tagging open data.

Study by Chaowaroj "Max" Wanotayaraj (KEK IPNS)

```
You will be running as vitis-ai-user with non-root UID/GID in Vitis AI Docker container

=====
Vitis-AI
=====

Docker Image Version: latest (CPU)
Vitis AI Git Hash: 6a9757a
Build Date: 2023-06-26
WorkFlow: pytorch

vitis-ai-user@cef02:/workspaces
```

Vitis-AI within docker

```
root@xilinx-vck190-20222:~/03_vck190_pytorch_atlas_top_tagger# python3 app_mt.py
XAIEFAL: INFO: Resource group Avail is created.
XAIEFAL: INFO: Resource group Static is created.
XAIEFAL: INFO: Resource group Generic is created.
inf> Starting 1 threads...
inf> Throughput=17749.99 fps, total frames = 1000, time=0.0563 seconds
inf> Accuracy= (856/1000)=0.856
root@xilinx-vck190-20222:~/03_vck190_pytorch_atlas_top_tagger#
```

ATLAS top tagging open data

```
root@xilinx-vck190-20222:~/Vitis-AI/examples/vai_library/samples/classification# ./test_video_classification_resnet18_pt 0 -t 8
[ WARN:0] global /usr/src/debug/opencv/4.5.2-r0/git/modules/videoio/src/cap_gstreamer.cpp (1081) open OpenCV | GStreamer warning: C
annot query video position: status=0, value=-1, duration=-1
XAIEFAL: INFO: Resource group Avail is created.
XAIEFAL: INFO: Resource group Static is created.
XAIEFAL: INFO: Resource group Generic is created.
WARNING: Logging before InitGoogleLogging() is written to STDERR
I1119 10:18:38.351377 1517 demo.hpp:752] DPU model size=224x224
I1119 10:18:38.392418 1517 demo.hpp:752] DPU model size=224x224
I1119 10:18:38.433463 1517 demo.hpp:752] DPU model size=224x224
I1119 10:18:38.474534 1517 demo.hpp:752] DPU model size=224x224
I1119 10:18:38.515609 1517 demo.hpp:752] DPU model size=224x224
I1119 10:18:38.556699 1517 demo.hpp:752] DPU model size=224x224
I1119 10:18:38.598032 1517 demo.hpp:752] DPU model size=224x224
I1119 10:18:38.639214 1517 demo.hpp:752] DPU model size=224x224
```

Camera video processing in DPU

```
(vitis-ai-pytorch) vitis-ai-user@cef02:/workspaces$ python run_quantize.py calib
[VAIQ_NOTE]: Loading NNDCT kernels...
[VAIQ_NOTE]: OS and CPU information:
  system --- linux
  node --- cef02
  release --- 6.2.0-26-generic
  version --- #26-22.04.1-Ubuntu SMP PREEMPT_DYNAMIC Thu Jul 13 16:27:29 UTC 2
  machine --- x86_64
  processor --- x86_64
[VAIQ_NOTE]: Tools version information:
  GCC --- GCC 9.4.0
  python --- 3.7.12
  pytorch --- 1.12.1
  vai_q_pytorch --- 3.0.0+a44284e+torch1.12.1
[VAIQ_NOTE]: GPU information:
  device name --- NVIDIA GeForce GT 1030
  device available --- True
  device count --- 1
  current device --- 0
[VAIQ_NOTE]: Quant config file is empty, use default quant configuration
[VAIQ_NOTE]: Quantization calibration process start up...
[VAIQ_NOTE]: =>Quant Module is in 'cuda'.
[VAIQ_NOTE]: =>Parsing MLP...
[VAIQ_NOTE]: Start to trace and freeze model...
[VAIQ_NOTE]: The input model MLP is torch.nn.Module.
[VAIQ_NOTE]: Finish tracing.
[VAIQ_NOTE]: Processing ops... | 9/9 [00:00<00:00, 8949.4
[VAIQ_NOTE]: =>Doing weights equalization...
[VAIQ_NOTE]: =>Quantizable module is generated.(./build/quant_model/MLP.py)
[VAIQ_NOTE]: =>Get module with quantization.
inf> Epoch 1: accuracy (test) : 42989/50000 = 85.97799682617188
[VAIQ_NOTE]: =>Exporting quant config.(./build/quant_model//quant_info.json)
```

Quantization with GPU

- Progress so far:
 - Study on fundamental elements.

PAM4

- Tested with QSFPDD.
- Customized protocol.

PCIe

- Tested with PCIe-CPM.
- Event readout and exchange logic.
- Belle II PCIe40

AI engine

- Design flow.
- Tested with many algorithms.

DPU

- Working environment with VCK190.
- GPU quantization.
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Plan for the next step

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- Forward-Error-Correction

- CPPM Marseille group: PCIe400 upgrade.
- Joint study on DMA development.
- Readout test with ADC card of SuperKEKB with WhiteRabbit

- Generalized plan on methodology.
- Implement various kinds of experimental (ATLAS/Belle II) algorithm

- Hardware extension
- Implement various kinds of experimental (ATLAS/Belle II) algorithm

New board: UT5

- Hardware spec. under discussion.
- Will start to make schematic and have a preliminary version in 2025.

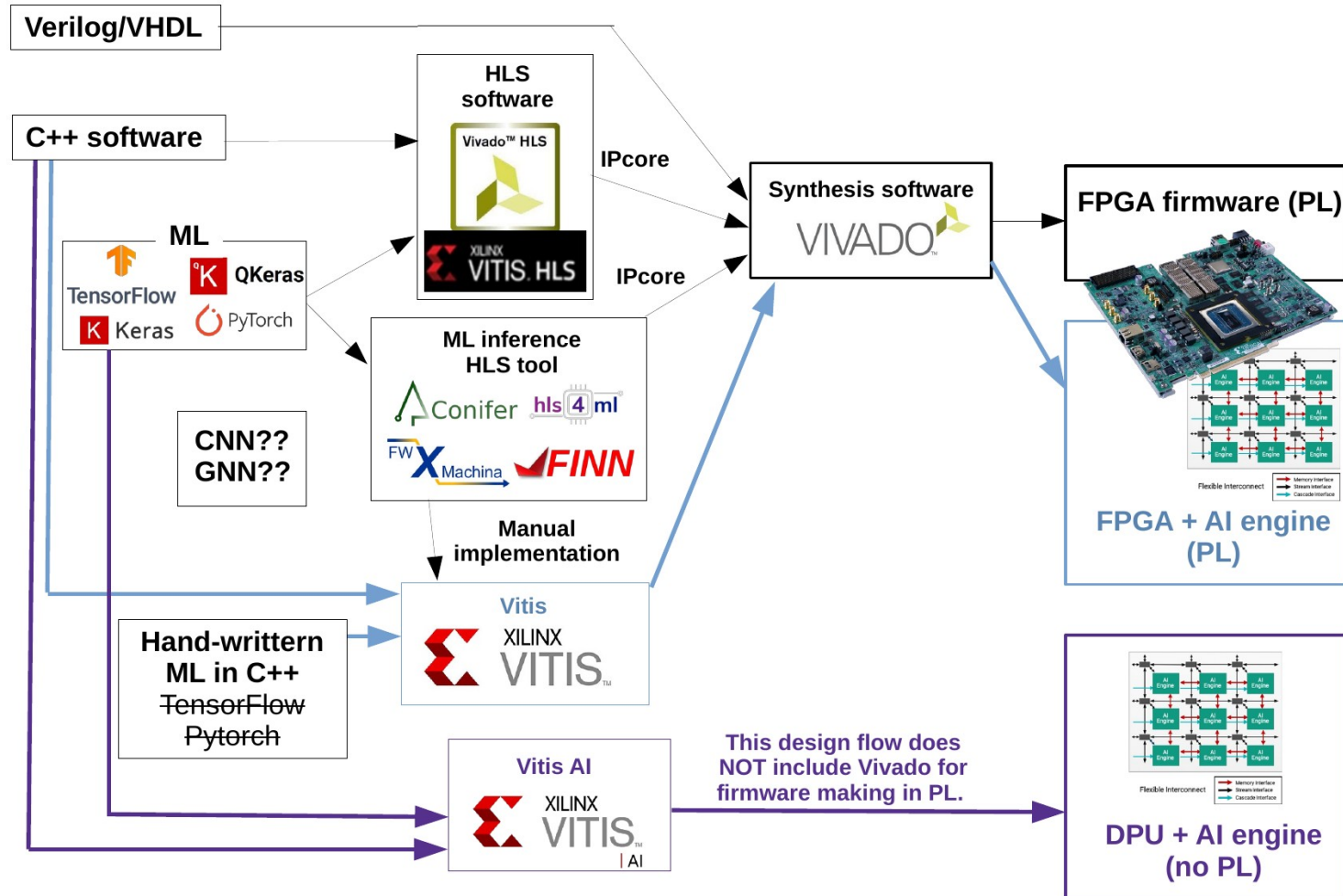
Algorithm making in FPGA: HLS, ML, AI engine

- Next step, we have many algorithms from Belle II, ATLAS, or so, to play in Versal kits.
 - Before that, let's think about the methodologies to do so.
- Considering algorithm implementation:
 - HDL logic in firmware.
 - HLS: software → firmware.
 - ML inference
 - AI engine.

} Depend on the different targets, our selection on FPGA differs. A strong FPGA? ACAP with AI engine? DPU?
- Not only the hls4ml, HLS tools has much more for ML and non-ML application.
 - Similarly, Versal AI engine requires a different design flow to make software/firmware.
- For this part of the work, we generalize the work plan into a roadmap in a technical perspective.

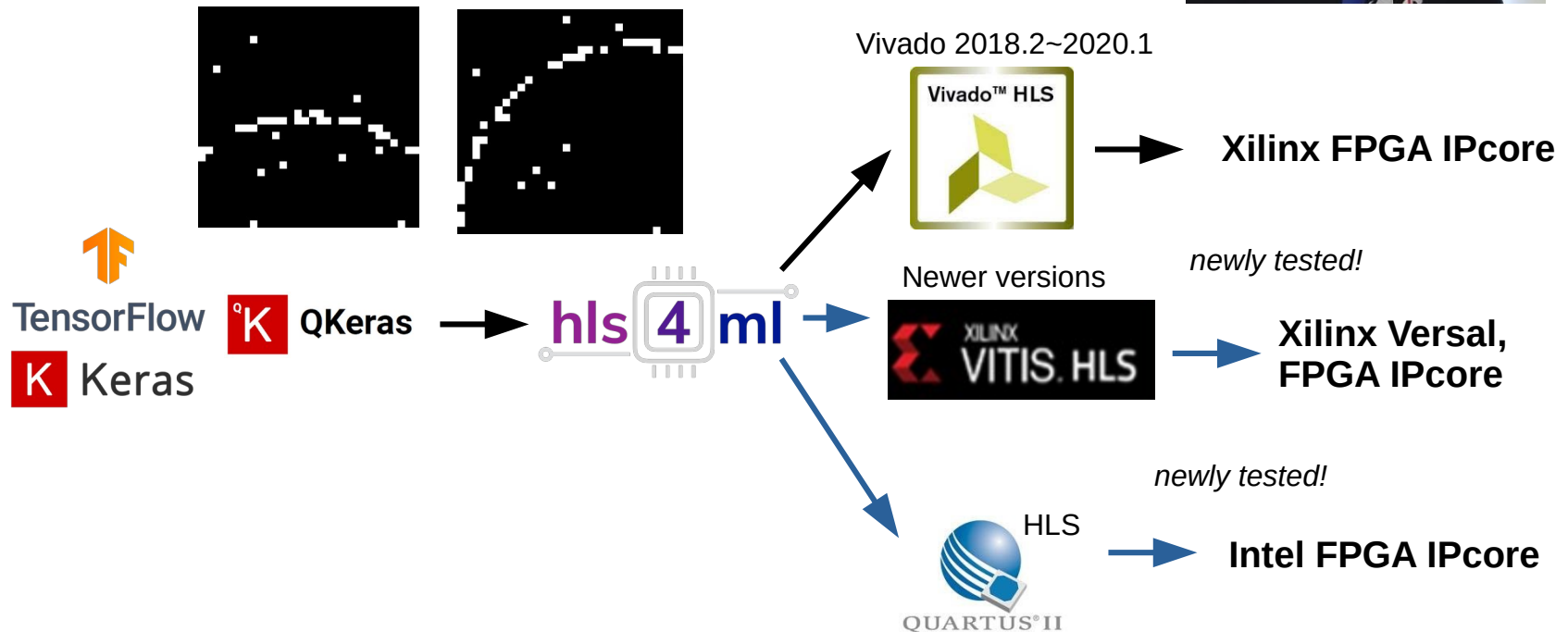
HLS, ML, AI engine: roadmap

- As a member of KEK E-sys group, we hope to understand the basic utilization on each, and build a database of such technical knowledge, to support our experimental colleagues.
- We are recruiting young student to learn/work with us.
- We also plan to make a series of hand-on lecture for each of them.



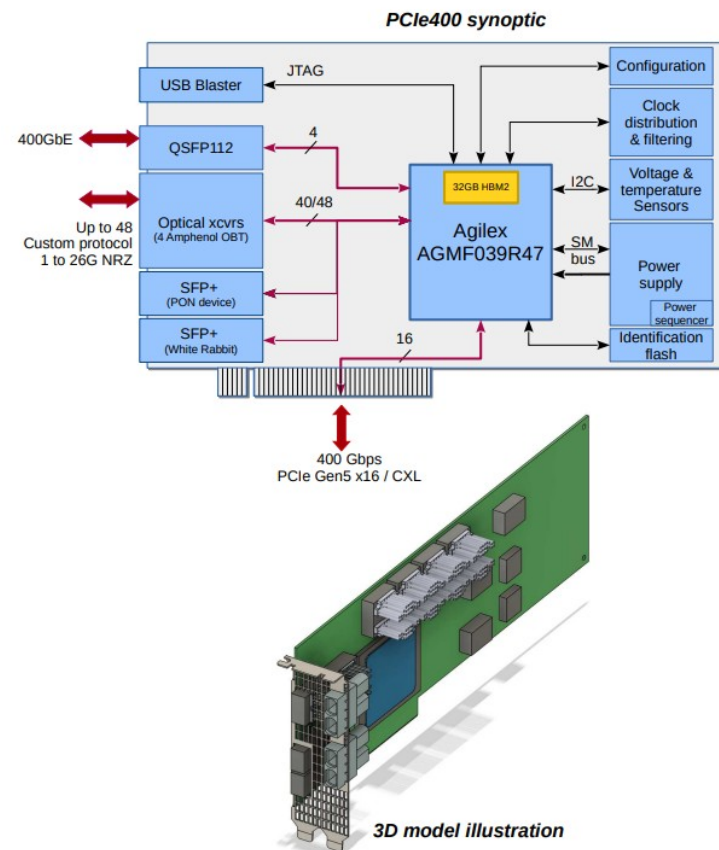
hls4ml

- hls4ml: A package for machine learning inference in FPGA.
 - Already lots of utilizations with Vivado HLS in Belle II and ATLAS.
- Yiyang Ding, our summer internship student in 2023, performed general studies on it.
 - A NN model for simple tracker and tested with VPK120!
 - Also tested with Intel FPGA with Quartus.
 - A manual has been prepared.



CPPM Marseille group: PCIe400 development

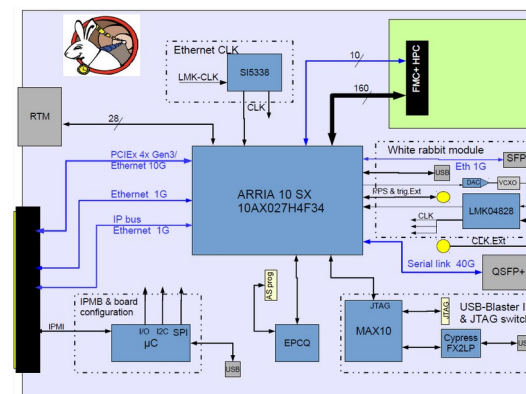
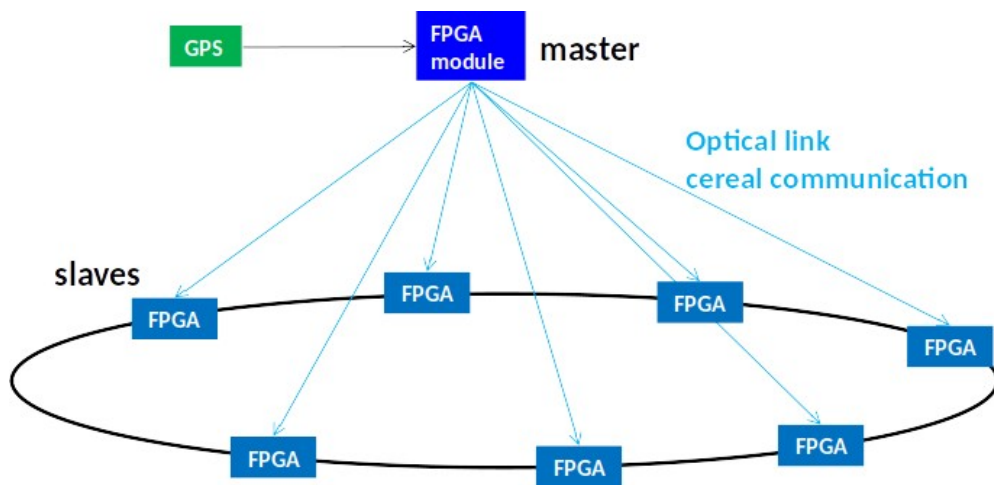
- PCIe400: next generation of readout board
 - Intel Agilex.
 - PCIe Gen5 x 16.
 - Planning for LHCb upgrade.
- Collaboration with CPPM Marseille:
 - Joint study on the PCIe DMA based readout firmware logic and driver software development.
 - PCIe40, PCIe400, and Versal boards.



source: CPPM Marseille group

WhiteRabbit system and IDROGEN module

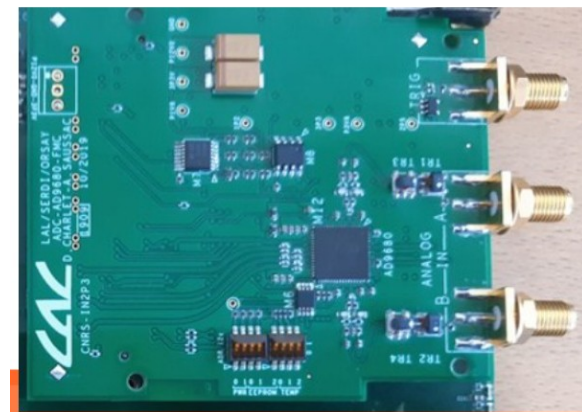
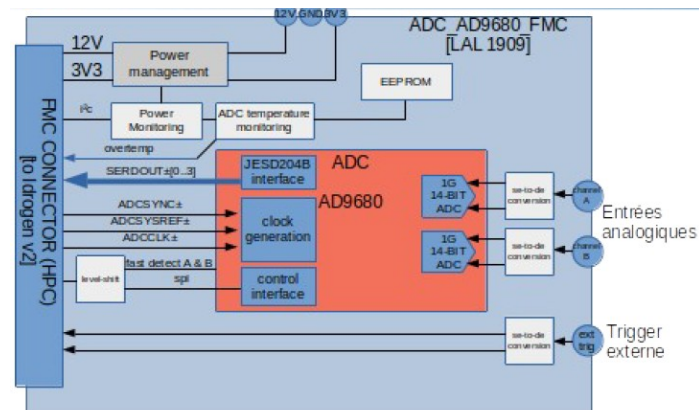
- WhiteRabbit: clock synchronizaion system
 - PTP (IEEE 1588)
 - Synchronous Ethernet
 - Recovery clock technology
 - Digital Dual Mixer Time Difference
 - Phase detection and compensation: Only WhiteRabbit
- Accuracy of synchronization: < 100ps
- IDROGEN: developed at IJCLab, SuperKEKB plans to use it.
 - Synchronization < 20ps
 - jitter < 1ps



accelerator beamline
~1km - 10km

ADC card with IDROGEN

- Main features:
 - ADC 9680, 2 channels, 14bits
 - 500 MS/s, 2GHz bandwidth
 - Wxternal trigger
 - Synchronization & timing by WhiteRabbit
- Triggerless application: on-going work
 - 4 x 250MS/s, 16bits
 - Free running with WhiteRabbit timestamping
- Collaboration:
 - Utilize our PCIe readout systems (PCIe40, Versal kits, etc) with DMA, and perform continuous data readout test to validate the ADC card data.



UT5 for Belle II and ATALS based on Versal

- Our final target: R&D of a universal device based on Versal.
 - A L1 trigger device is almost expected:
- Discussion on the hardware spec. is ongoing.
 - Plan to make preliminary version of circuit schematic in 2025.

Belle II UT3



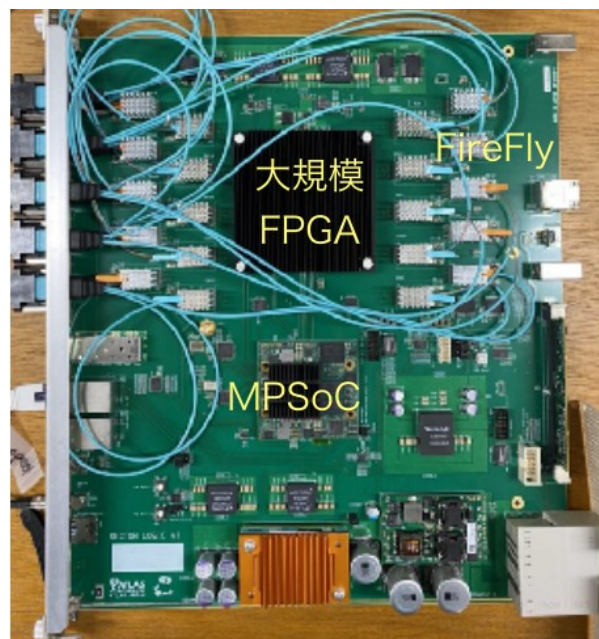
Xilinx Virtex-6
xc6vhx380t, xc6vhx565t
11.2 Gbps with 64B/66B

Belle II UT4



Xilinx UltraScale
XCVU080, XCVU160
25 Gbps with 64B/66B

ATLAS Muon Trigger processor



Xilinx UltraScale+
XCVU13P XCZU5EV
GTH,GTY: 16.8 Gbps
with 64B/66B

Summary

- 2023: We studied many fundamental functionalities of the Xilinx Versal ACAP devices.
- 2024: Further studies on those functionalities, algorithm development in FPGA, and circuit design on the UT5.
 - CPPM Marseille, SuperKEKB: newly collaborated.

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