Overview of ALICE Inner Tracking System: Current Performance and Future Upgrade

Jiyoung Kim¹ on behalf of the ALICE collaboration

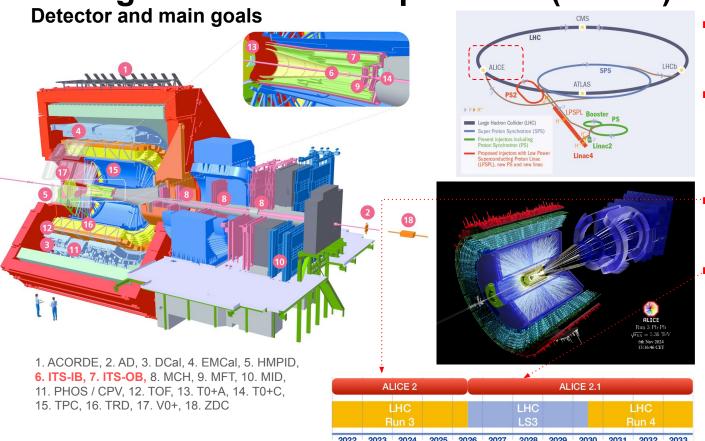
The 29th International Nuclear Physics Conference
30, May 2025
DCC, Daejeon, Korea







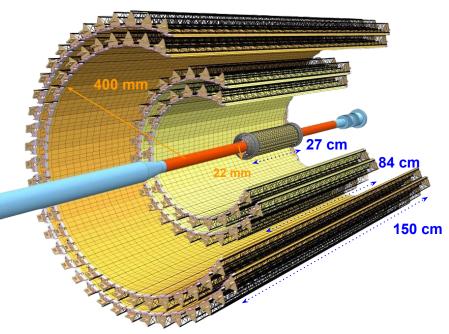
A Large Ion Collider Experiment (ALICE)



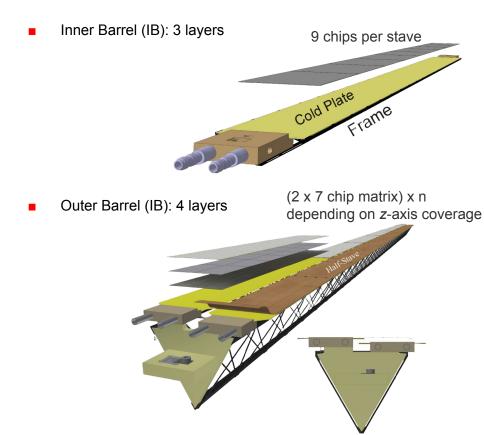
- Study of Quark-Gluon Plasma (QGP) created in heavy ion collisions at the LHC
- Reconstruction of charm and beauty hadrons

 ⇒ High resolution and low mass inner tracker close to the beam point
 - Inner Tracking System (ITS) has been updated from ITS1 to ITS2 and operating since 2022
 - R&D of the next upgrade (ITS3) is ongoing. It will be installed during LHC Long Shutdown 3

ITS2 detector layout

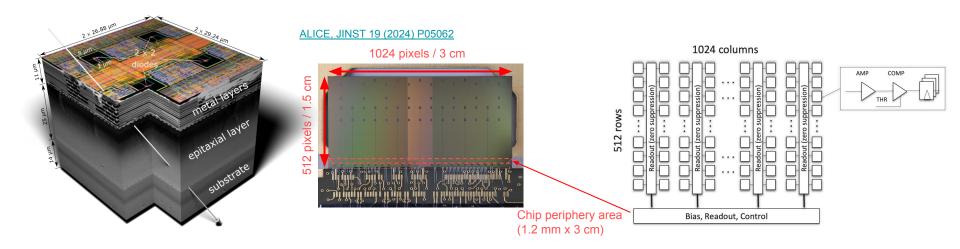


- Vertexing and track reconstruction
- 7 layers
- Radius from interaction point: 22 mm 400 mm
- Water cooling system

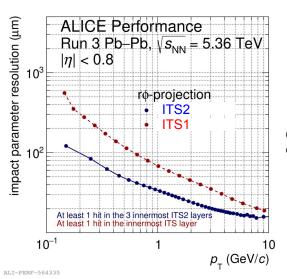


ALICE Pixel Detector "ALPIDE" - the pixel chip for the ITS2

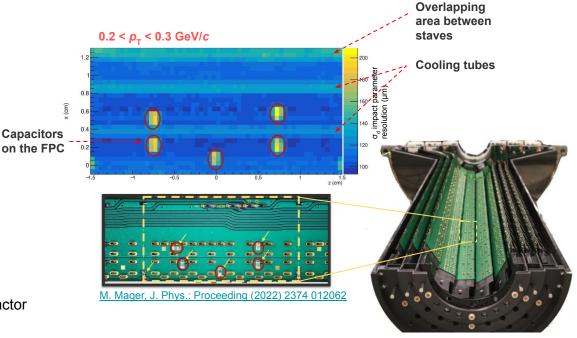
- TowerJazz 180 nm CMOS Imaging Sensor Process
- Pixel pitch: 29 μm x 27 μm
- Highly integrated circuit: O(100) transistors in-pixel:
 - Analog and digital signal processing, control and readout functionalities
- Maintain detection efficiency (> 99%) and fake-hit rate (< 10⁻⁶ /pixel/event) beyond a Total Ionizing Dose (TID) of 270 kRad and Non-Ionizing Energy Loss (NIEL) of 2.7 × 10¹² 1 MeV n_{eq}/cm²



Impact parameter resolution

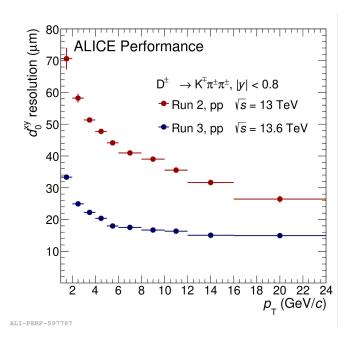


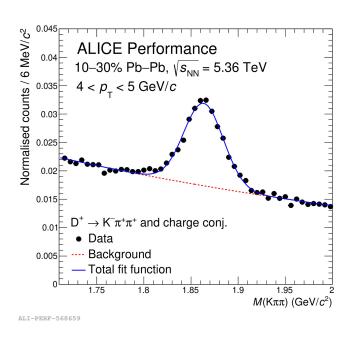
Compared to the previous ITS1, ITS2 shows enhanced impact parameter resolution by a factor of more than 2 for particles with p_{τ} < 1 GeV/c



- Details being studied:
 - Detailed material composition of the first layer clearly visible
 - Improving detector description in simulations

Physics performance

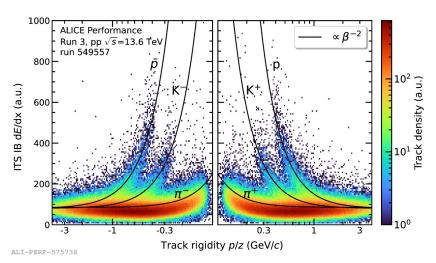




- Measurement of impact parameter with charmed D[±] mesons ($c\tau \sim 300 \mu m$)
 - Factor 2-5 improvement in impact parameter resolution compared to Run 2 (ITS1) with Run 3 (ITS2)
- Improvement of the reconstruction of weak-decaying particles in Pb–Pb



Particle identification with ALPIDE - ITS Color run

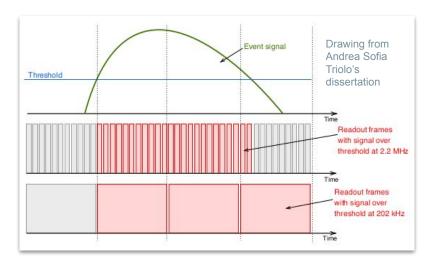


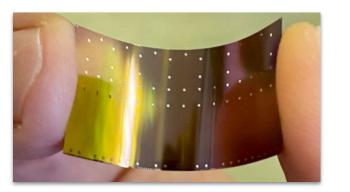
- - Only feasible at low Interaction rate in p-p
 - High readout rate (2.2 MHz)

Detector parameters during color run

- Deactivation of signal clipping
 - In the nominal operation, the signal is clipped to avoid double counting of hits from the same particle

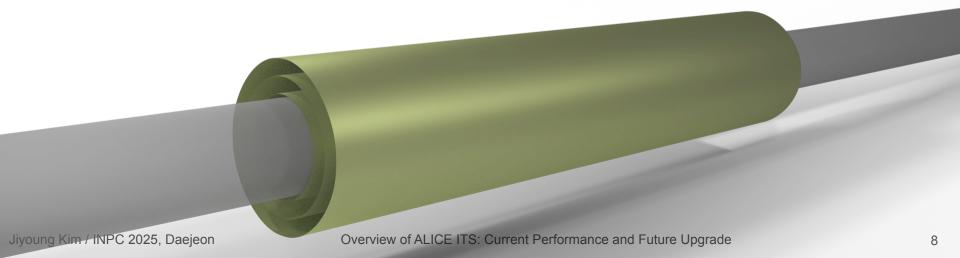
- Usage of Time over Threshold (ToT) information to access the particle energy loss in the ALPIDE sensitive layer
- Proof of concept of dE/dx measurement with binary readout MAPS
- Oversampling with increased the framing rate to obtain the ToT information proportional to the deposited charge







Future upgrade: ITS3



ITS3 upgrade - key concept

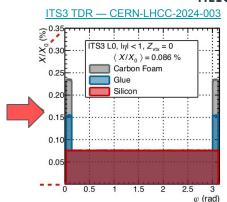


Other
Water
Carbon
Aluminum
Kapton
Glue
Silicon
mean = 0.35 %

0.1

0.0

Azimuthal angle [*]



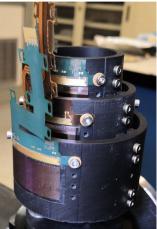
- Replacement of ITS2 Inner Barrel with 3 layers of curved, 50 um thick, wafer-scale MAPS
- Air cooling & ultra-light mechanical supports
- Reduced material budget of on average:
 0.36 % X₀ per layer → 0.09 % X₀ per layer
- Smaller radius of the innermost layer:

23 mm → **19 mm**

- Key items in R&D
 - Bending of silicon wafer
 - Stitching
 - Air cooling







Stitched wafer-scale MAPS

ALICE

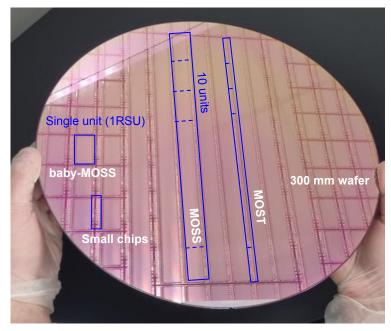
- Engineering Run 1
 - First MAPS for HEP using stitching
- Monolithic Stitched Sensor (MOSS):

14 x 259 mm, 6.72 MPixels (22.5 x 22.5, 18 x 18 µm²)

- Conservative design
- Different pitches
- Monolithic stitched Sensor Timing (MOST):

2.5 x 259 mm, 0.9 MPixels (18 x 18 µm²)

- More dense design
- Power segmentation
- Baby-MOSS (single stitch ~ reticle-sized)
- Plenty of small chips (like MLR1)



Multi-Layer reticle 1

Engineering Run 1

Engineering Run 2

Engineering Run 3

The state of the s

Validated 65 nm CIS TPSCo process

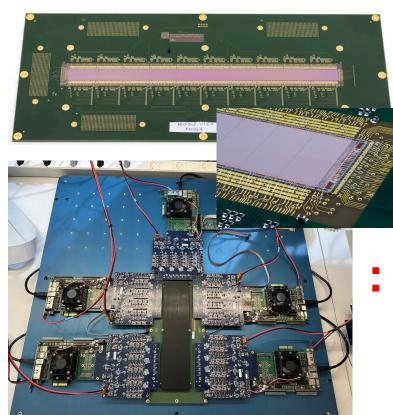
First submission of large-scale stitched MAPS

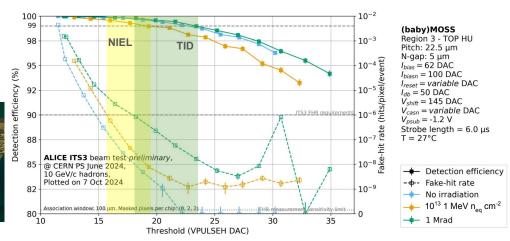
Specifications close to final ITS3 sensor

Final sensor to be used in ITS3



Stitched wafer-scale MAPS – MOSS – latest results

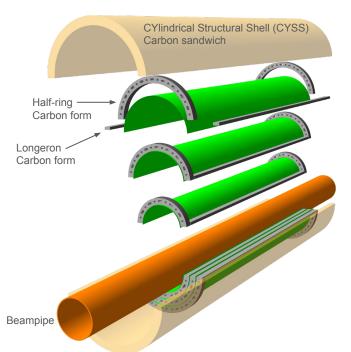


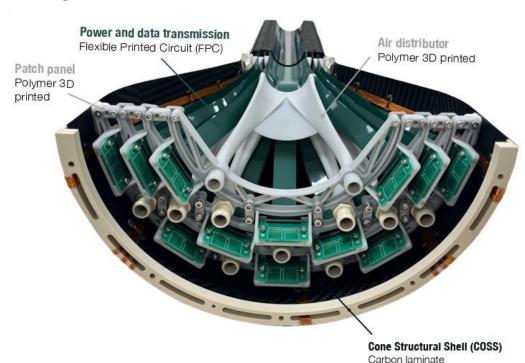


Detailed characterisation at the laboratory and at test beam

Operational margin (efficiency > 99% and fake-hit rate < 10^{-6} /pixel/event) is maintained at the ALICE radiation levels, 400 krad and 4 \times 10¹² 1 MeV n_{eq} cm⁻²

Mechanical support and integration test





- The R&D of mechanical supports and air cooling is ongoing in parallel with sensor development
- Engineering model has been produced and performed the integration test

Summary and outlook



- ITS2 has demonstrated excellent performance
 - Impact parameter resolution and reconstruction of weakly-decaying secondary particles
 - Successful color run demonstration for particle identification capability
- R&D of ITS3 upgrade under preparation
 - Replacement of 3 innermost layers with curved, ultra-light, wafer-scale MAPS
 - Characterized the first stitched wafer-scale sensor
 - Mechanical support and cooling study ongoing in parallel
- **Next steps:** Full functionality prototype chip (ER2) is expected to come in the end of 2025. Stay tuned!







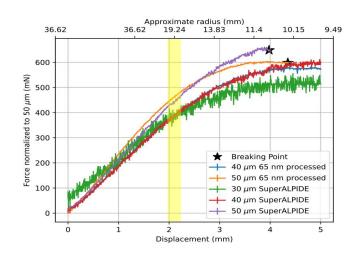


Backup

ALIC

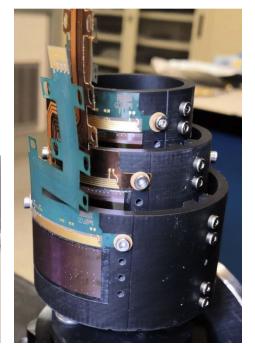
ALPIDE chip bending test

- Bending test with diverse thicknesses → Very Flexible. Fully bent to 19 mm
- Beam tests of bent chip at DESY
 - Bent MAPS feasibility demonstrated for the first time
 - Important milestone in the R&D for ALICE ITS3
- Demonstration of fully bent sensor on FPCB is done as well

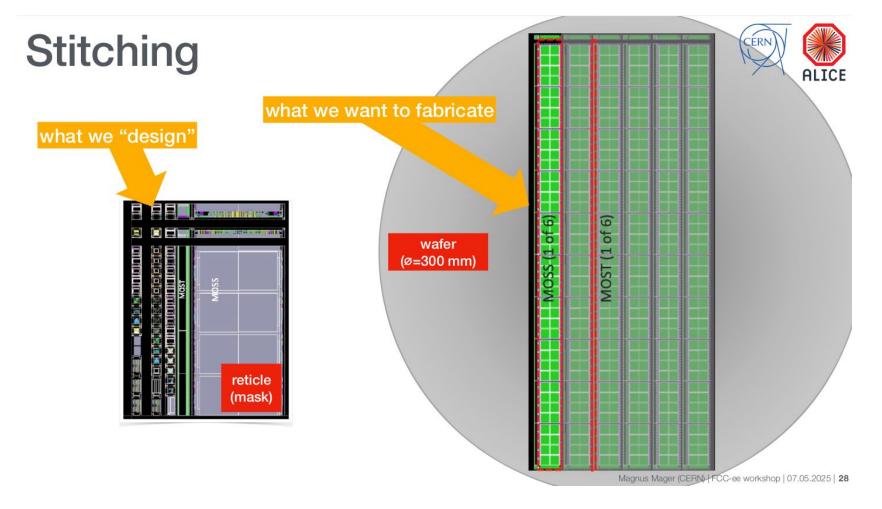


ITS3 TDR — CERN-LHCC-2024-003 j.nima.2021.166280 arXiv:2502.04941

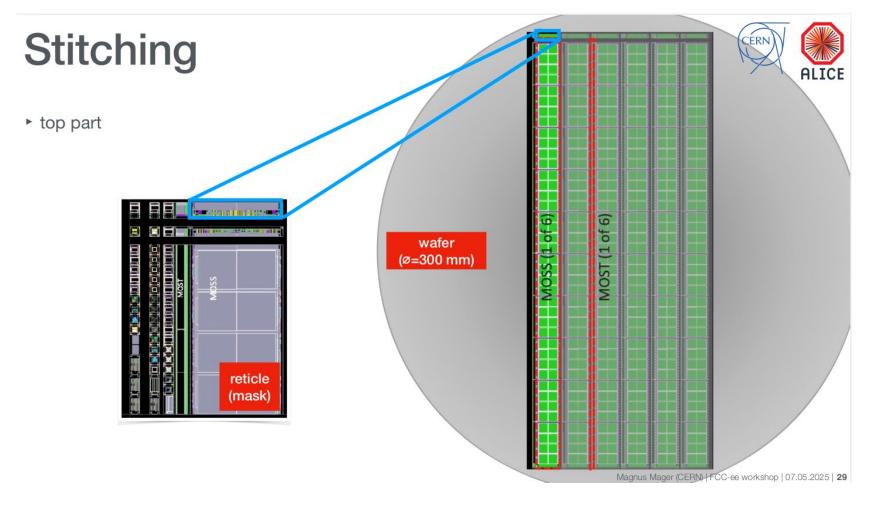




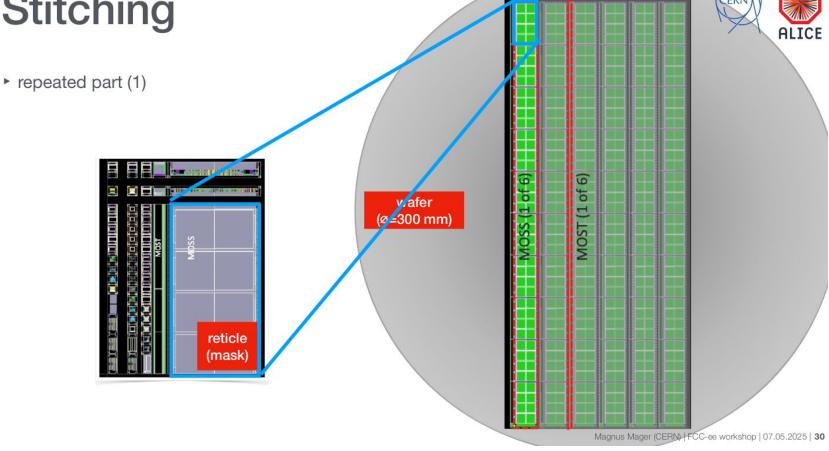




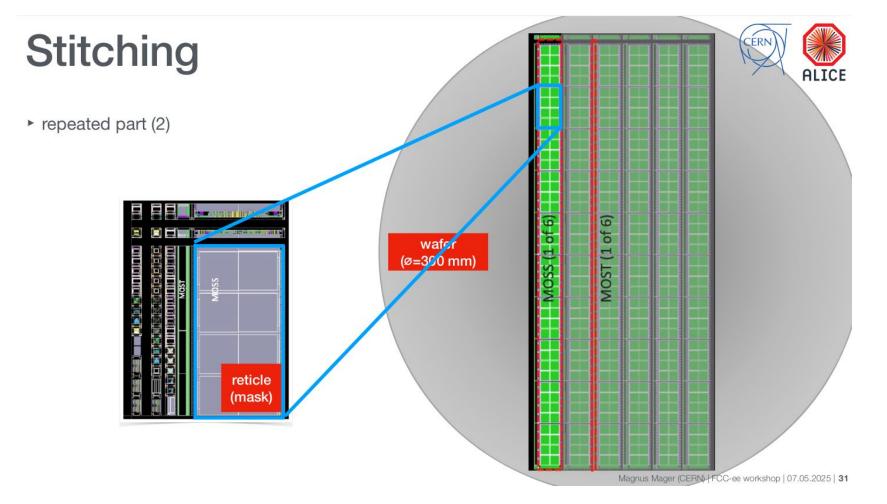




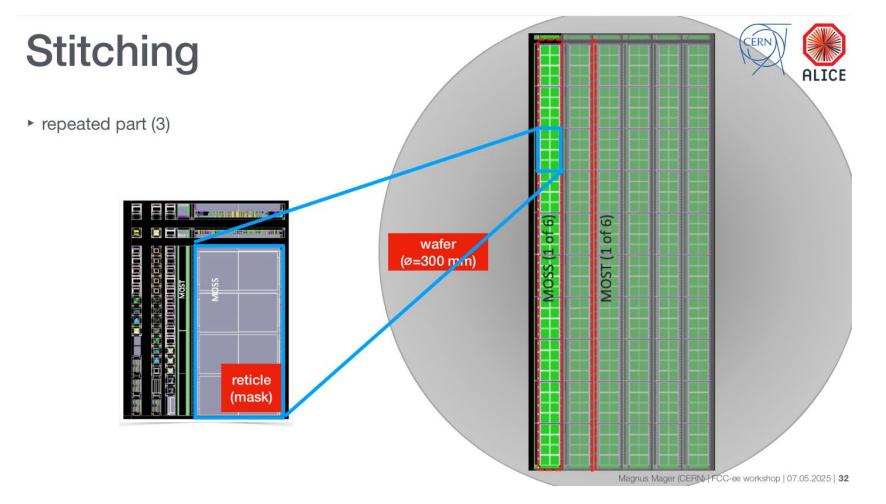








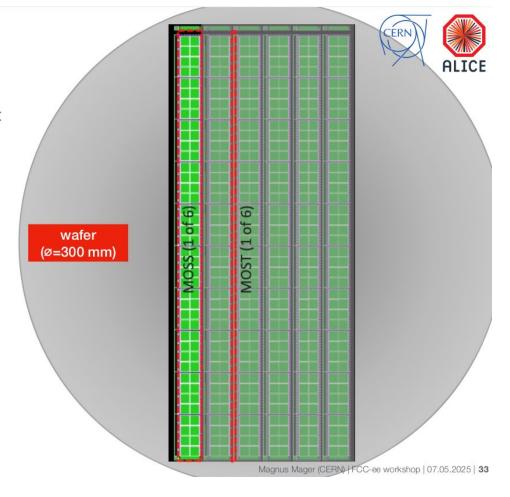




Stitching

final circuit is a concatenation of different parts of the masks

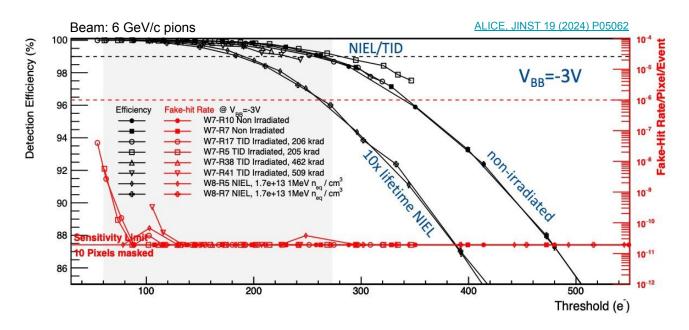








Detection efficiency and fake-hit rate of non-irradiated and irradiated ALPIDEs



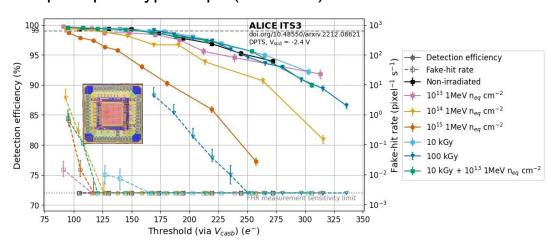
- Detection efficiency ~ Charge collection performance
- Fake hit rate/pixel/event ~Noise level
- Efficiency drops according to higher threshold values as expected
- Operational margin
 - > 99 % efficiency
 - < 10-6 fhr/pixel/event</p>
- After high-does irradiation, ALPIDE keeps high efficiency and low noise level based on ample operating margin
- Nominal operating point is at 100 e-

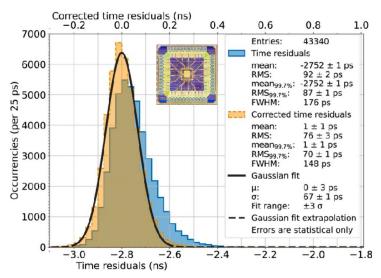
Process modification: 10.1016/j.nima.2017.07.046

APTS paper: <u>arXiv:2403.08952</u> DPTS paper: <u>NIM A.2023.168589</u> Time resolution: <u>arXiv:2407.18528</u>



- pixel prototype chips (selection)





- Multi-Layer Reticle 1 (MLR-1): common effort by ALICE ITS3 and CERN EP R&D
 - Various small scale prototypes with pixel matrices and ancillary circuitry
 - ► Technology explored far beyond the requirements of ITS3 in terms of radiation hardness and time resolution
 - ⇒ Promising also for future applications like ALICE 3 Vertex Detector and FCC-ee

Multi-Layer reticle 1

Engineering Run 1

Engineering Run 2

Engineering Run 3



The next chip baseline specifications





Parameter	ALPIDE (existing)	Wafer-scale sensor (this proposal)
Technology node	180 nm	65 nm
Silicon thickness	50 μm	20-40 μm
Pixel size	27 x 29 μm	O(10 x 10 μm)
Chip dimensions	1.5 x 3.0 cm	scalable up to 28 x 10 cm
Front-end pulse duration	~ 5 μs	~ 200 ns
Time resolution	~ 1 μs	< 100 ns (option: <10ns)
Max particle fluence	100 MHz/cm ²	100 MHz/cm ²
Max particle readout rate	10 MHz/cm ²	100 MHz/cm ²
Power consumption	40 mW/cm^2	< 20 mW/cm ² (pixel matrix)
Detection efficiency	> 99%	>99%
Fake-hit rate	< 10 ⁻⁷ event/pixel	< 10 ⁻⁷ event/pixel
NIEL radiation tolerance	$\sim 3 \times 10^{13} \text{ 1 MeV } n_{eq}/\text{cm}^2$	$10^{14} 1 \text{ MeV } n_{eq}/\text{cm}^2$
TID radiation tolerance	3 MRad	10 MRad

ALPIDE is a great starting point, samller technology node will open further possibilities!

Magnus Mager (CERN) | Sensor development for the ALICE ITS upgrade in LS3 | DAQFEET-2021 | 08.02.2021 | 22



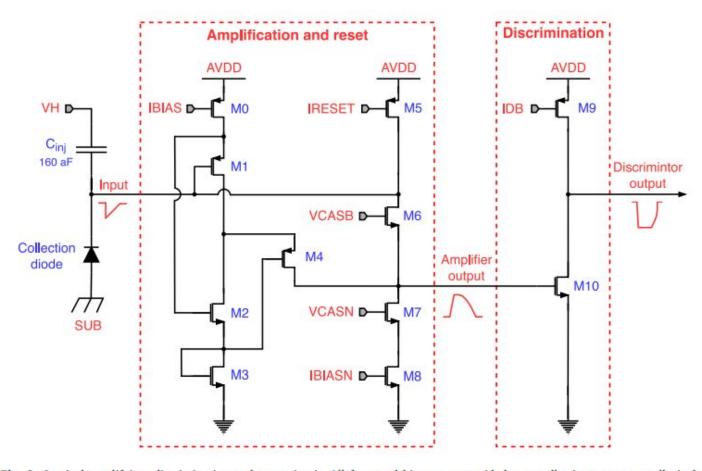


Fig. 3. In-pixel amplifying, discriminating and reset circuit. All front-end biases are provided externally, in common to all pixels.



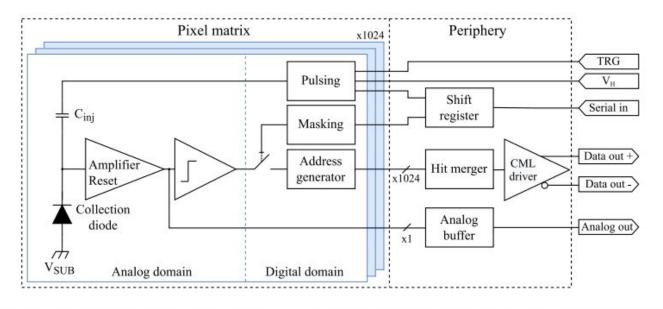
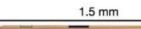
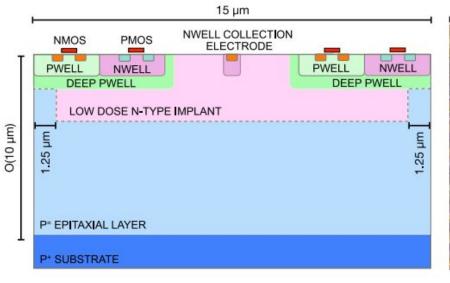
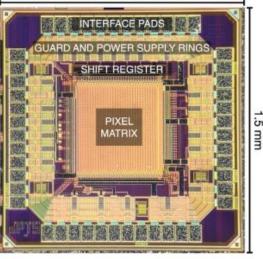


Fig. 2. DPTS functional diagram. 1024 pixels can be masked from readout and selected for pulsing via a shift register. The addresses of hit pixels are read out via a differential digital output line. The in-pixel amplifier output of a single pixel is connected to an interface pad.









(a) Pixel cross section. Not to scale.

(b) Chip under microscope.

Fig. 1. A cross section of a DPTS pixel and a photo of the chip under a microscope.



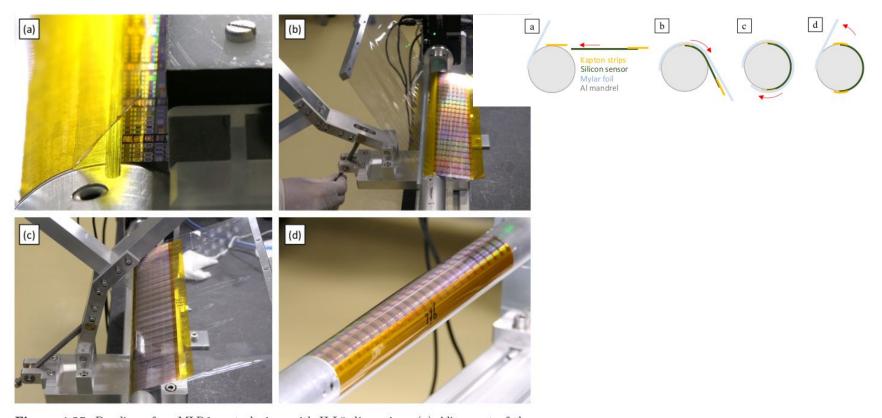
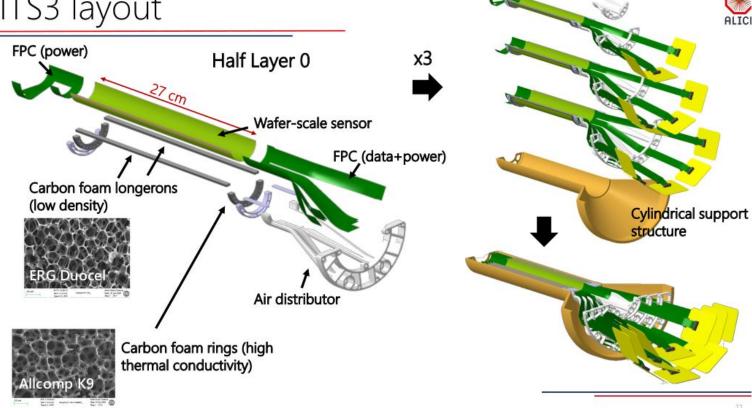


Figure 4.35: Bending of an MLR1 central piece with H-L0 dimension. (a) Alignment of the half-layer, (b) start of the bending procedure, (c) half-layer during bending and (d) bent.

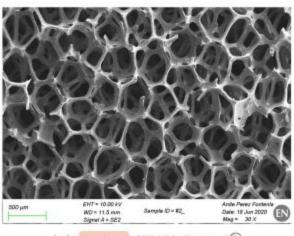


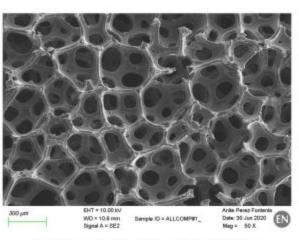
ITS3 layout

ITS3 layout









(a) Carbon (RVC) Duocel®

(b) Allcomp K9 standard density

Figure 4.6: Microscopy images of the carbon foams used in ITS3 cooling system. The two images have different scales.